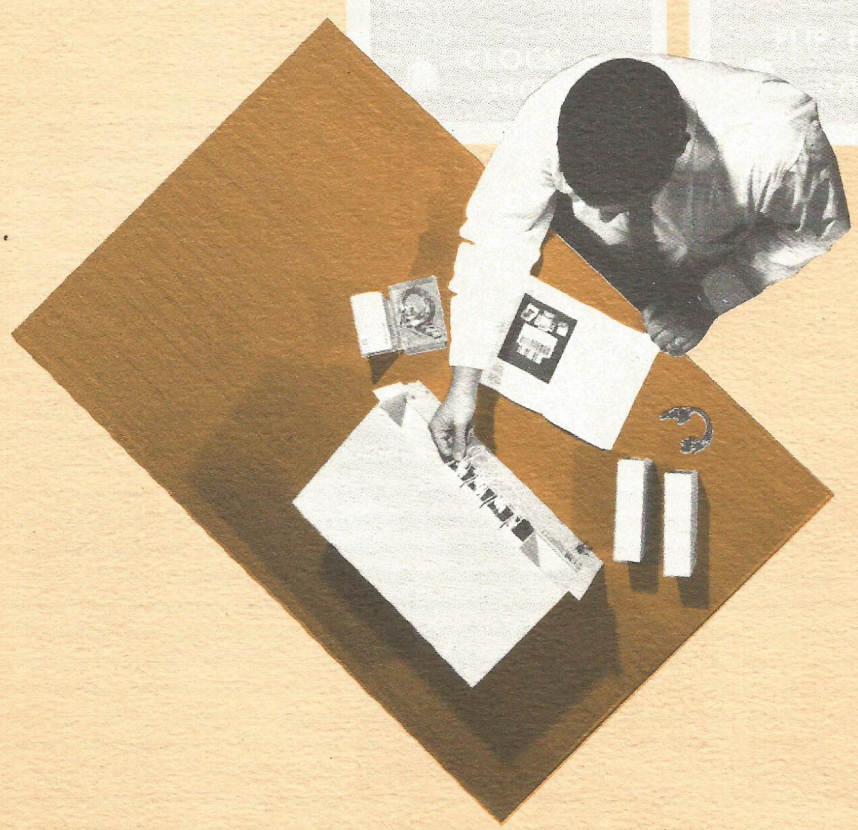
LEARNING

• *Digital Computer Logic* • *Logical Design*

• *Systems Development* • *Test Techniques*

with the . . .

DIGITAL LOGIC KIT



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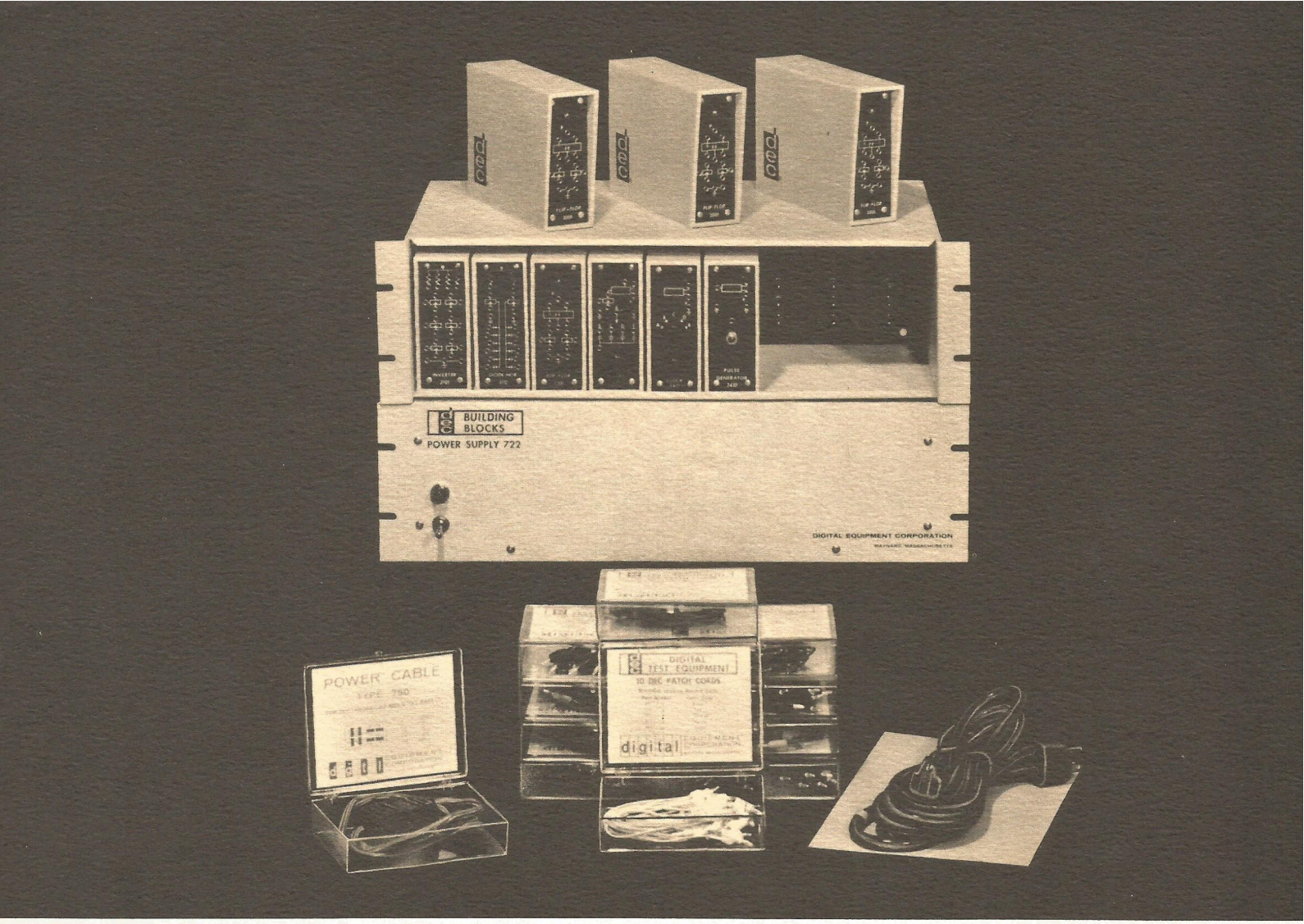


DEC's Digital Logic Kit provides a means of learning and testing digital techniques and developing logical systems. Composed of reliable, commercially manufactured equipment, the Logic Kit is ideally suited for educational and industrial training as well as practical digital systems test and design work.

The Logic Kit consists of a fully coordinated set of completely transistorized digital computer circuits packaged in convenient "building block" form. All the necessary equipment needed to perform a variety of classroom demonstrations and laboratory experiments is included.

By utilizing various combinations of circuit modules provided in the kit, one can individually construct and test a variety of logical circuitry — i.e. up counters, down counters, four-bit shift registers, Gray-to-binary decoders, two-binary-digit adders and subtracters, etc.

For ease of instruction, all modules are furnished with graphic front panels indicating their logical function.

One need only select the required modules, plug them into the mounting panel and make the necessary interconnections. All logical interconnections can be made quickly and easily by means of handy stacking banana-jack patch cords which are inserted directly into the face of the panel. Units can be assembled and reassembled in any number of different combinations. Power connections are automatically made when the module is plugged into the mounting panel.

The Logic Kit is equipped with modules which operate at any speed from DC up to 500 kilocycles. The selection of this particular speed range has been designed to permit maximum economy without loss of quality and reliability. Where greater speed is required however, these versatile units may be combined with and are fully compatible with other Digital speed lines in the 5 megacycle and 10 megacycle range.

Included in the Logic Kit are nine modules — one inverter, one diode nor, four flip-flops, one delay, one clock, and one pulse generator — and the necessary accessory equipment — power supply, power cable, mounting panel, and one hundred patch cords.

Digital's versatile "building block" concept affords the instructor and design engineer alike, maximum flexibility. As more advanced techniques are reached, the Logic Kit can be supplemented as needed with a variety of special purpose circuitry. A wide selection of fully compatible modules are available in all three speed ranges. Price of the complete Logic Kit (FOB Maynard) is $1022.

We shall be pleased to send you upon request a free copy of our "Module Catalog" which describes in detail the more than 200 different modules available for your use.

A small rectangle with an enclosed solid triangle is an inverter.

INVERTER

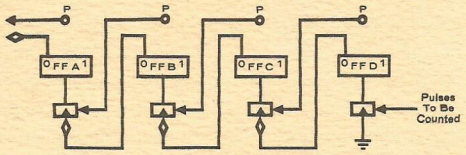
A resistor with a large solid dot is a standard DEC clamped load resistor.

CLAMPED LOAD

The solid diamond is a logic level for which the assertion level is −3 volts.

LEVEL — NEGATIVE

The open diamond logic level for which assertion level is grou



UP COUNTER

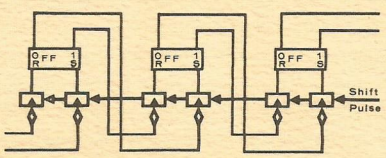
Figure 1

COUNTING SEQUENCE

0	0000	4	0100	8	1000	12	1100
1	0001	5	0101	9	1001	13	1101
2	0010	6	0110	10	1010	14	1110
3	0011	7	0111	11	1011	15	1111

A typical method for building a flip-flop counter is shown in Figure 1. Pulses enter from a pulse generator or a clock, and each input pulse will trigger flip-flop D. If flip-flop D is in the ONE state when the input pulse arrives, a carry pulse will be generated to flip-flop C. If flip-flop C is in the ONE state and is triggered, another carry pulse will be generated to trigger flip-flop B. When this process is continued down a line of flip-flops, a carry chain is formed.

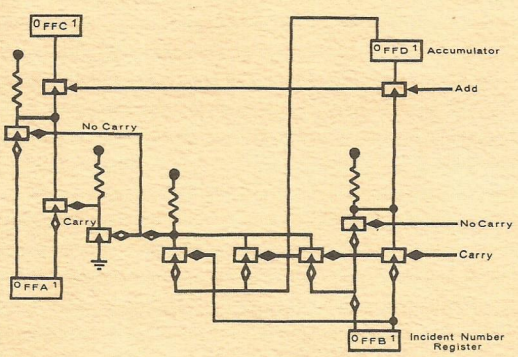
The carry pulses are generated by ANDing together the ZERO level output from a flip-flop and the P pulse output from the same flip-flop in an inverter. For example, if flip-flop D is in the ONE state and receives a trigger pulse, a similar pulse will appear at its pulse output and this pulse will pass through the inverter gate into flip-flop C. To assure that the output of flip-flop D will not change state until the pulse is completed, a delay has been built into each flip-flop package. The contents of the flip-flop counter may be read by means of the indicator lights on the front panel.



SHIFT REGISTER

Figure 2

Figure 2 shows a typical shift register using the jam transfer method. Associated with each flip-flop are two inverters used as AND gates. The set flip-flop input is activated by a shift pulse which is conditioned by the ZERO output of the previous flip-flop: the reset input, by the ONE output. Thus the contents of the previous flip-flop are jammed into the next flip-flop. The delay built into the flip-flop output amplifiers prevents the output from changing state until the sampling pulse is ended.



ADDER

Figure 3

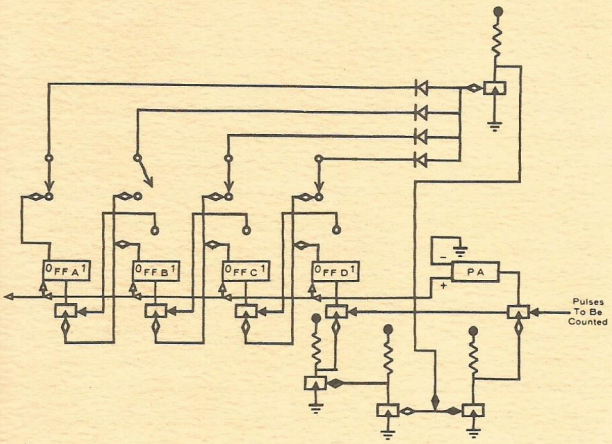
A straightforward parallel adder may be constructed using the Type 3201 flip-flop, as illustrated in Figure

3. The contents of the incident number register (flip-flop A and B) are added to the contents of the accumulator (flip-flop C and D). A new sum (in the accumulator) and a carry (if applicable) are produced. In order to make the addition process complete, provision must be made for a possible carry from the previous stage of the adder, as shown.

The table below lists all possible combinations to be considered in the addition process.

Incident Number	Accumulator	Carry In	Accumulator after add (sum)	Carry Out
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

→ LEVEL — GROUND	The solid arrowhead is a negative pulse (from ground).	→ PULSE — NEGATIVE	The open arrowhead is a positive pulse (from ground).	→ PULSE — POSITIVE	Arrowheads (or diamonds) are used at all branch points to indicate signal flow.		



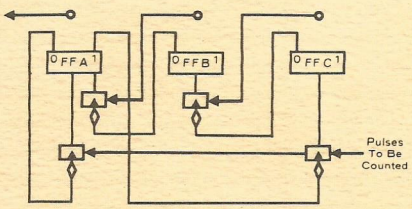
SPECIAL COUNTER

Arbitrary count — count of 12 illustrated

Figure 4

Often it is desirable to build a counter that will produce a signal after a particular number (N) of events have occurred. If N is an integer power of 2, the output is automatically produced by the final digit of a counter of appropriate length. If N is not a power of 2, gating must be performed to detect the desired number, generate a signal, and reset the counter to 0. Diode gates may be used to sense the number N-1, close the input to the counter, and re-route the Nth input pulse so that it will clear the counter and generate an output signal. This is a completely general method which will work for any value of N.

The system in Figure 4 counts to 12. On the 11th count the NOR gate activates its inverter which in turn closes the counter to the incoming 12th pulse and connects the circuitry that will permit the pulse amplifier to clear the counter on the 12th pulse.



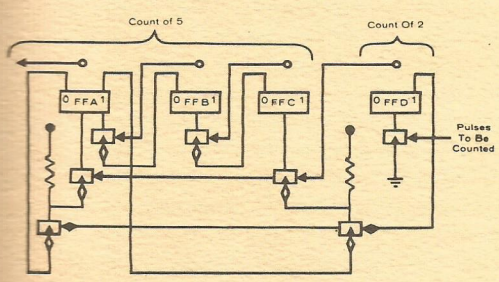
COUNTING SEQUENCE	
0	000
1	001
2	010
3	011
4	100

BINARY CODED DECIMAL COUNTERS

Count of 5

Figure 5

A typical counting sequence is shown N=5 in Figure 5. The progress of the count is shown in the table. When the count of 4 is reached, the next pulse will clear the counter and generate an output signal.

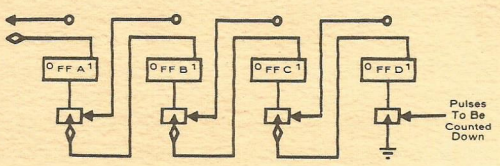


COUNTING SEQUENCE	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Count of 10

Figure 6

From the simple count-of-5 circuit, binary coded decimal counters may be generated. To give a count of 10, the counter for 5 is preceded by a binary counter (Figure 6).

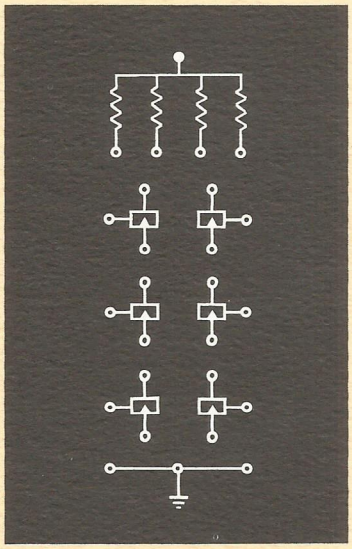


DOWN COUNTER

Figure 7

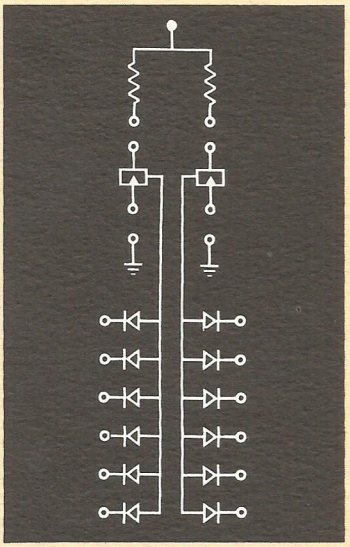
In a down counter, each successive pulse will decrease the count by 1. The method for building a down counter is essentially the same as that used in the up counter, except that each flip-flop input is conditioned by the ONE output of the previous flip-flop. In this way, the Pulse chain will form a high-speed borrow circuit instead of a carry circuit.

LOGIC MODULES

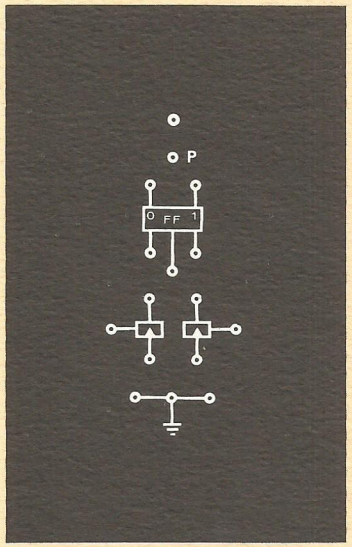


INVERTER — Type 3101 — A simple transistor gating circuit similar in function to a mechanical switch. When the base input terminal of the transistor is at −3 volts, the transistor is saturated and the emitter is shorted to the collector.

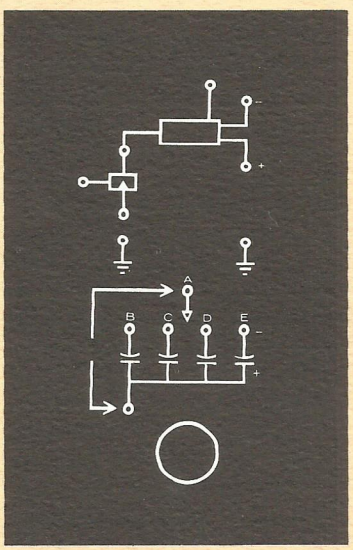
When the base input terminal is at ground, the transistor is cut off and the emitter-to-collector path is open. Price $47.



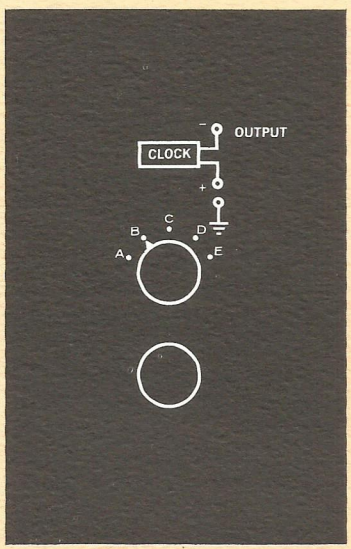
DIODE NOR — Type 3110 — Contains two circuits, each with six inputs. Each circuit acts as an OR gate for negative levels or pulses and as an AND gate for ground levels. The output is ground if one or more inputs are negative; it is negative if all inputs are positive or not connected. Price $43.



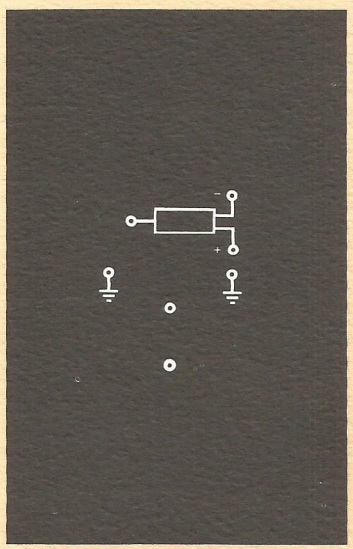
FLIP-FLOPS — Type 3201 — Bistable storage elements each capable of retaining one bit of information. When a "Set" input is introduced, the flip-flop is placed in the ONE state. The ONE output terminal will be at −3 volts, and the ZERO output will be at ground. When a "reset" input is applied, the flip-flop is placed in the ZERO state. The ZERO output terminal will then be at −3 volts, and the ONE output will be at ground. A "Complement" input reverses the state of the flip-flop. Price $63.



DELAY — Type 3301 — Produces a level of variable duration at one output terminal, followed by a single pulse at the other output terminal. The duration of the level delay is variable. Price $74.

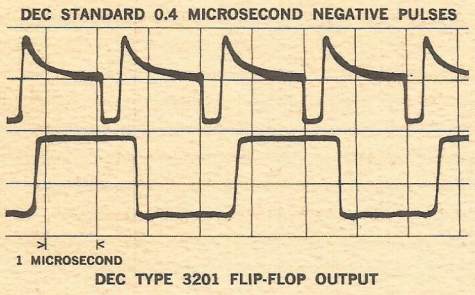


CLOCK — Type 3401 — Produces standard pulses at variable repetition frequencies. (Crystal clocks are available for constant pulse repetition frequencies.) Price $67.



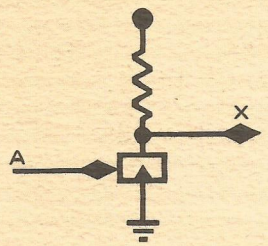
PULSE GENERATOR — Type 3410 — Used to initiate action. It will produce a standard pulse at the command of a push button or as the result of a negative-going level change. Price $41.

ELECTRICAL CHARACTERISTICS



All modules in the Logic Kit use the same three power voltages (−3 volts, −15 volts and +10 volts). This allows any arrangement of modules in the Mounting Panel. Power connections permit convenient marginal checking. The DEC Pulse used with this speed range is 2.5 volts in amplitude and 0.4 microsecond in width. The DEC Standard Levels are ground and −3 volts. These levels are used for all logical operations in both high-speed and low-speed lines.

LOGICAL CHARACTERISTICS



In DEC modules, logical operations are performed by combinations of saturable transistor inverters. The user can consider these as simple switches. In the graphic symbology used with the DEC modules, a negative level on the input A (base of the transistor inverter) will "short" the output X (collector) to ground, while a ground level on A will "open" the gate, and the output will be −3 volts. "AND" circuits and "OR" circuits are formed by putting transistors in series or in parallel. A DEC Flip-flop is set by "shorting" the appropriate input to ground through a pulse gate.

MECHANICAL CHARACTERISTICS

All circuits are dip soldered and mounted in aluminum cases measuring 1¾ x 4½ x 7 inches. Nine units can be accommodated in the standard 5″ x 19″ x 7″ Mounting Panel. Power wiring is factory installed in the Mounting Panel.

ACCESSORIES

POWER SUPPLY Type 722	Supplies three Standard voltages of −3 volts, −15 volts and +10 volts for a typical assortment of 45 modules. Price $305.
POWER CABLE Type 750	Cable with matching plug for Type 901 Mounting Panel. Price $3.
MOUNTING PANEL Type 901	Will hold nine DEC modules. Has built-in filters, and can be used in rack or on bench. Price $100.
PATCH CORDS Type 911	Miniature stacking banana jacks. Come in color-coded lengths of 2, 4, 8, 16, and 32 inches. In bundles of 10. Price $9.

OTHER DEC PRODUCTS

In addition to the equipment described in this folder, Digital designs and manufactures general purpose, high speed, solid state digital computers and special systems including core and memory testers and memory exercisers. For information on these and other Digital products, contact Sales Department, Digital Equipment Corporation, Maynard, Massachusetts.

QUANTITY DISCOUNTS

$5,000 — 3%; $10,000 — 5%; $20,000 — 10%; $40,000 — 15%; $100,000 — 20%; $250,000 — 22%

All shipments are F.O.B. Maynard, and prices do not include state or local taxes. Prices and specifications are subject to change without notice.

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