Digital Processor LABEN 70

LABEN

Laboratori Elettronici e Nucleari

LABEN - Divisione della MONTEDEL - Montecatini Edison Elettronica S.p.A.

general features

memory

16-bit word size - 17th bit for parity option.

Capacity of 4096 expandable to 32.768 words.

Memory cycle time: 1.4 μsec

8 addressing modes and extended addressing.

basic LABEN 70

Comprehensive instruction set: 76 basic instructions + 1024 microprogrammed skip instructions.

10 registers all simultaneously displayed on console.

All arithmetic registers addressable as memory locations.

Two index registers (X and B).

input-output

Standard multilevel priority interrupt system.

Up to 128 external distinct levels for 64 peripheral devices.

Up to 32 high-speed simultaneous direct memory access channels, any of which may be assigned, by program, to any of peripheral devices.

Data channel instructions for high-speed sequential input/output to or from memory in interrupt mode

options

Hardware multiply and divide

Direct memory access channels

Memory protect

Real time clock

Power failure protection and restart system

software

Monitor for compiling, loading and executing on a mass storage

Relocating loader

Input/output control and interrupt processing

Assembler and Extended Assembler

ASA FORTRAN IV

Subroutines library

Debugging aids

Utility and diagnostics programs.

The LABEN 70 is the latest achievement in the evolution of LABEN's instrumentation line and represents the outcome of over ten years of experience in the design and production of advanced digital instrumentation for scientific research, space and industrial process applications.

— In the nuclear field, LABEN designs and produces a complete range of multichannel analyzers, wired-program computers, magnetic-core memory systems, and ADC converters widely used by outstanding Research Centres for nuclear spectrometry.

— LABEN's developments in the space research area include PCM telemetry systems of proven reliability in a number of space missions and ground data processing stations.

— LABEN is active in the design and production of digital data processing, telemetering and telecontrol systems for industrial applications. These systems are tested to provide optimum performances in the presence of electromagnetic disturbances in power plant control applications.

The wide experience gained in the design of large wired-program systems for scientific research, the advanced technologies employed to achieve high reliability in the equipment for space applications, the up-to-date approaches studied to assure immunity from electromagnetic disturbances in industrial instrumentation have provided the « HARDWARE » facilities for the development of the LABEN 70 computer.
To provide extensive support « SOFTWARE » capabilities, LABEN has engaged a selected group of specialists with a strong background in software problems.

foreword

specifications

memory and addressing

— Word size of 16 bits
— Memory expandable from 4 to 32 Kwords (4096-word module)
— One hardware index register, and second accumulator (B register) used as second index register.
— Eight addressing modes
— Single and double indexing
— Multilevel indirect addressing
— Extended addressing (single or double skip provided)
— Protected loader and resident monitor.

arithmetic

— Parallel two's complement binary

compute speed

— 1.4 µsec machine cycle
— 2.8 µsec add
— 2.8 µsec subtract
— 14 µsec multiply (with multiply/divide option)
— 15.4 µsec divide (with multiply/divide option)
— 700.000 words per second data transfer in cycle stealing mode
— 120.000 words per second data transfer in standard interrupt mode.

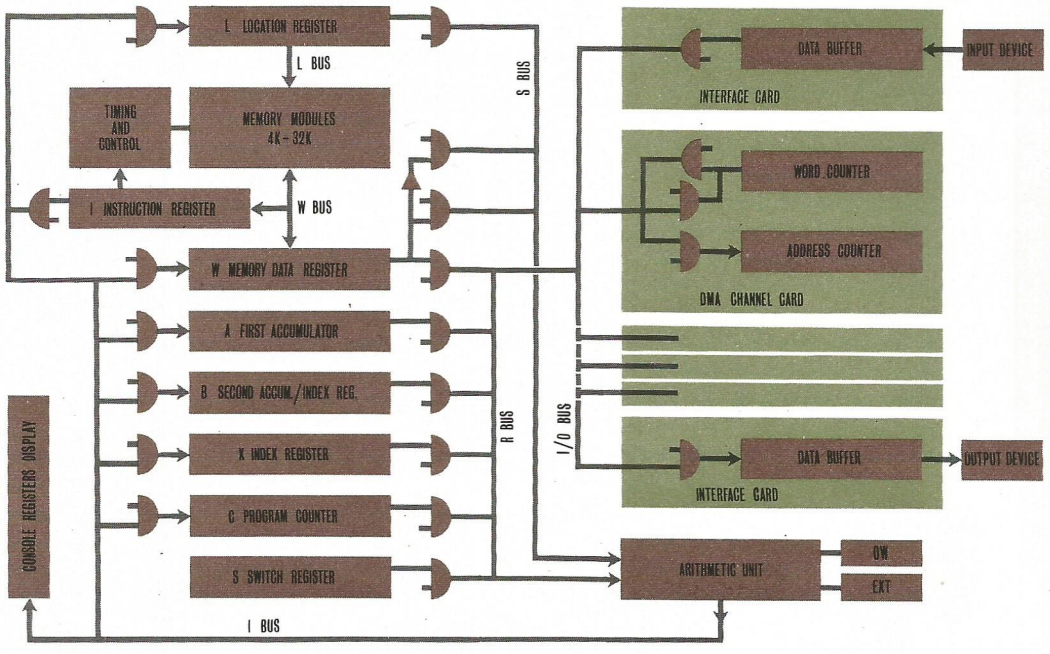
instructions

— Memory reference instructions: 30, also used as inter-register instructions.
— Skip instructions (microprogrammable): 512 single or double
— Shift instructions (shift count from 1 to 31): 24
— Input/output instructions:

- data transfer instructions	:	4	
- command or status transfer instructions	:	4	
- external control instructions	:	10	
- data channel instructions	:	4	
- Total		76	basic instructions
		1024	microprogrammed skip instructions

registers

— A accumulator addressable as location zero
— B second accumulator also used as index register; addressable as location one
— OW overflow register; 1 bit
— E extend register; 1 bit
— X index register; addressable as location two
— L location register
— C program counter
— W memory data register
— I instruction register: 16 bits
— S switch register, manually transferable to A, B, X, C, L or memory, addressable as location three.
— The arithmetic (A, B, X) and switch (S) registers addressable as normal memory location (zero to three) can generally be used in all memory reference instructions.



LABEN 70 computer block diagram

input-output

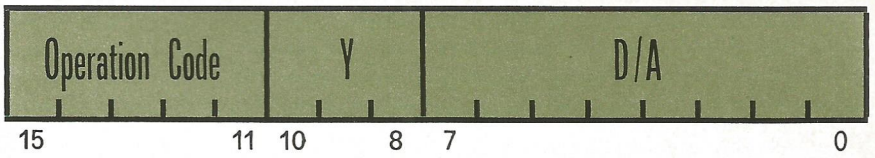
— Standard multi-level priority interrupt provides up to 128 external distinct levels for 64 peripheral devices, on a two levels per device basis. Further levels can be added for each device on request.
— Four additional levels are provided for internal use: parity check power failure, memory protect and memory overflow, console interrupt.
— Priority levels can be altered either manually, simply by interchanging the position of interface cards **without any need for software changes,** or dinamically under program control by masking any level.
— Up to 64 interrupt levels can use one of the four data channel instructions (see input/output instructions), thus enabling the peripheral devices to perform fast data transfer in interrupt mode at a maximum rate ranging from 120 to 180 Kwords per second, depending upon the data channel instruction type selected.
Two of the memory locations available are reserved to each level address and word counter.
— Fast data transfer modes relating to the four data channel input/output instructions:
- sequential input to memory per byte or word
- sequential output from memory per byte or word
- memory increment capability, especially suitable for amplitude spectra measurements with automatic displacement
- add to memory feature particularly useful in averaging measurements
— Up to 32 optional simultaneous direct memory access (DMA) channels can be added to basic configuration, any of which may be assigned, by program, to any of peripherals. Two hardware registers are provided within each channel for address and word counter.
— Four different types of data transfer in DMA mode for each channel may be selected by program:
- sequential input to memory: 700.000 words per second
- sequential output from memory: 700.000 words per second
- memory increment operation for amplitude spectra measurements
- add to memory operation for multiscaling and averaging measurements.

console control

— POWER ON, POWER OFF. Switch computer power on/off.
— RUN. Starts operation at the current machine state.
— HALT. Stops computer operation at the end of current cycle.
— STATUS RESET. Presets the computer to fetch phase, turns off interrupt system, resets Overflow, Extend, parity error, memory protect, and location overflow indicators.
— MAIN RESET. As « status reset », but registers are reset too.
— LOAD ADDRESS. Transfers Switch Register setting to C and L registers.
— LOAD A, LOAD B, LOAD X. Transfer Switch Register setting into A, B, or X register.
— EXAMINE. Displays the memory contents (location specified by L register) stored in W register and increments C register.
— DEPOSIT. Transfers Switch Register setting into memory (location specified by L register) and increments C register.
— DEPOSIT ENABLE. Must be depressed to enable DEPOSIT operation, thus preventing accidental memory data alteration.
— SINGLE CYCLE. Steps program one machine cycle.
— CONSOLE INTERRUPT. Interrupts running program thus transferring control to monitor program.
— LAMP TEST. Lights all console lamps for failure check.
— LOADER PROTECTED/OFF. Permits alteration of protected memory locations.
— MEMORY ENABLE/DISABLE. Inhibits memory operation preventing memory data alteration when power is switched off.

specifications

memory reference instructions



Word Formats

Y Addressing Mode

D/A Displacement/Address

In this format the operation code is followed by three address control bits.

These bits (8 : 10) specify:
direct/indirect addressing,
relative/absolute addressing,
indexing.

The process of actual address computation is summarized in Table 1. The symbols used are defined as follows:

A Address - Bits 0 through 7 in absolute value (range 0 through 255)

D Displacement - Bits 0 through 7 intended as an integer in two's complement form (range -128 through 127)

(A) Contents of location A

(D) Contents of location D

(C) Contents of C register (the address of the instruction)

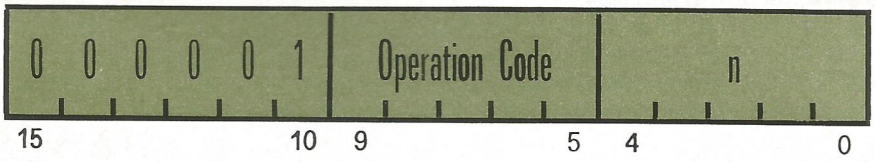
(X) Contents of X index register

(B) Contents of B index register

Table 1 - Actual Address Computation

Y	Actual Address	Comments
000	A	Direct absolute to « base page » (location 0-255)
001	(A)	Indirect absolute
010	(C) + D	Direct relative
100	(C) + D + (X)	Direct relative to X register
110	(C) + D + (X) + (B)	Direct relative to X and B registers
011	(C) + (D)	Indirect relative
101	(C) + (D) + (X)	Indirect relative to X register
111	(C) + (D) + (X) + (B)	Indirect relative to X and B registers

Mnemonic	Description	Cycles
LDA	Load A	2
LDB	Load B	2
LDX	Load X	2
DLD	Double Load AB	3
STA	Store A	2
STB	Store B	2
STX	Store X	2
DST	Double Store AB	3
ADA	Add to A, result in A	2
ADB	Add to B, result in B	2
ADX	Add to X, result in X	2
SBA	Substract from A, result in A	2
SBB	Substract from B, result in B	2
SBX	Substract from X, result in X	2
ANA	And to A, result in A	2
ORA	Or to A, result in A	2
ERA	Ex-or to A, result in A	2
ANM	And to A, result in memory	3
ORM	Or to A, result in memory	3
ERM	Ex-or to A, result in memory	3
MUL	Multiply	11
DIV	Divide	12
JMP	Jump	1
JMS	Jump to subroutine	2
XEC	Execute	1
CSE	Compare memory with A and skip if equal	3
ISZ	Increment memory and skip if zero	3
CPL	Complement	3
CLR	Clear	3
DSZ	Decrement memory and skip if zero	3

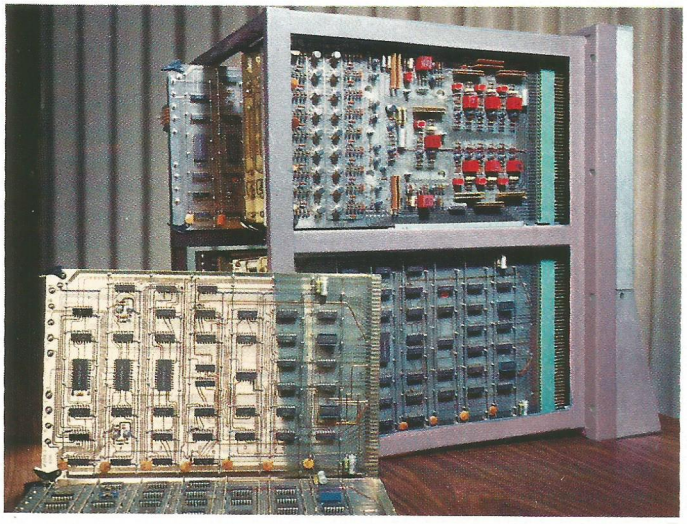


shift instructions

n = Shift count (1 to 31)

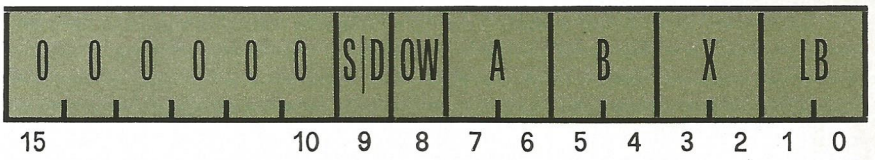
Mnemonic	Description	Cycles
ALA	Arithmetic Shift A Left	1+O. 125n
ARA	Arithmetic Shift A Right	1+O 125n
ALB	Arithmetic Shift B Left	1+O. 125n
ARB	Arithmetic Shift B Right	1+O. 125n
ALX	Arithmetic Shift X Left	1+O. 125n
ARX	Arithmetic Shift X Right	1+O. 125n
LLA	Logical Shift A Left	1+O. 125n
LRA	Logical Shift A Right	1+O. 125n
LLB	Logical Shift B Left	1+O. 125n
LRB	Logical Shift B Right	1+O. 125n
LLX	Logical Shift X Left	1+O. 125n
LRX	Logical Shift X Right	1+O. 125n
RLA	Rotate Shift A Left	1+O. 125n
RRA	Rotate Shift A Right	1+O. 125n
RLB	Rotate Shift B Left	1+O. 125n
RRB	Rotate Shift B Right	1+O. 125n
RLX	Rotate Shift X Left	1+O. 125n
RRX	Rotate Shift X Right	1+O. 125n
ADL	Arithmetic Double Shift Left	1+O. 125n
ADR	Arithmetic Double Shift Right	1+O. 125n
LDL	Logical Double Shift Left	1+O. 125n
LDR	Logical Double Shift Right	1+O. 125n
STO	Set Overflow bit °	1
STE	Set Extend bit °	1

° Overflow and Extend instructions are coded under Shift Group.



skip instructions

(512 possible combinations, simple and double)



Word Format

S/D Specifies that the skip must be simple or double

OW Specifies the conditions for the Overflow bit.

A,B,X, Specify the conditions for the contents of A, B and X

LB Specifies the conditions for Extend bit (E), Least Significant bit of X (X_0) and B (B_0) registers.

The conditions that can be tested by the fields OW, A, B, X, and LB are shown in the tables below.

OW	Skip Condition
1	no condition
0	(OW) = 0

A	Skip Condition
11	no condition
00	(A) $\neq$ 0
01	(A) $\geqslant$ 0
10	(A) $\leqslant$ 0

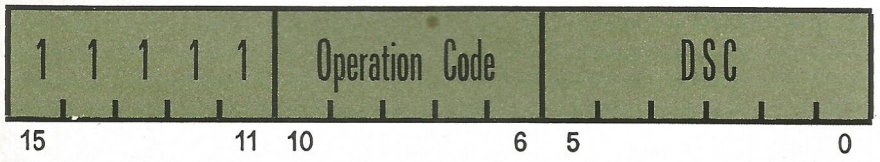
LB	Skip Condition
11	no condition
00	(X_0) = 0
01	(B_0) = 0
10	(E) = 0

The B and X fields specify the same conditions as the A field, but referred to the contents of B and X registers.

The above individual conditions can be combined to form a compound condition which is the AND of the specified conditions. In this way the user can specify up to five conditions. When the compound condition is satisfied and bit 9 (S/D) is equal to zero, the next memory location is skipped; if bit 9 is equal to one, the next two memory locations are skipped.

The number of cycles required to execute a compound skip instruction is equal to the number of operative conditions specified by fields A, B, and X. If none of these conditions is specified, the number of cycles is always equal to one.

Mnemonic	Description	Cycles
OWF	Overflow bit equal zero	1
ANE	(A) Not Equal zero	1
AGE	(A) Greater or Equal zero	1
ALE	(A) Less or Equal zero	1
BNE	(B) Not Equal zero	1
BGE	(B) Greater or Equal zero	1
BLE	(B) Less or Equal zero	1
XNE	(X) Not Equal zero	1
XGE	(X) Greater or Equal zero	1
XLE	(X) Less or Equal zero	1
LBA	(A_0) Equal zero	1
LBB	(B_0) Equal zero	1
EXB	(E) Equal zero	1



input-output instructions

The first field (bits 15÷11) contains a fixed code (37_8) characteristic of this group of instructions.
DSC (Device Selector Code) indicates the name (number) of the peripheral unit concerned with the imput/output instruction.
In the « operation code » bits 6 and 10 are used to identify four categories.

Basically Input/Output instructions fall into four main categories:

- *data transfer instructions*
- *command or status transfer instructions*
- *external control instructions*
- *data channel instructions*

data transfer instructions

Mnemonic	Description	Cycles
OTA	Output from A to selected device	1
* OTM	Output from Memory to selected device	2
INA	Input to A from selected device	1
* INM	Input to Memory from selected device	2

Operation Code Format and Notes

Operation code: 0XXY0

X, X designate the 4 instructions

Y - indicates whether during instruction flag is reset or not.

* OTM and INM instructions leave unchanged the A, B, and X registers and Extend and Overflow bits.

command or status transfer instructions

RSA	Read status (of selected device) to A and reset temporary conditions of status word	1
RSM	Read status (of selected device) to Memory and reset temporary conditions of status word	2
WSA	Write status (command) from A to selected device	1
WSM	Write status (command) from Memory to selected device.	2

Operation code: 0XXY1

X, X

Y - see data transfer instructions

external control instructions

CLF	Clear flag of selected device	1
STF	Set flag of selected device	1
SKF	Skip if flag of selected device is clear	2
STC	Set control flip flop enabling selected device to operate in interrupt mode	1
CLC	Clear control flip flop disabling selected device to operate in interrupt mode	1
SKC	Skip if control flip flop is clear	2
EMA	Enable selected device to operate in direct memory access	1
EIS	Enable interrupt system	1
DIS	Disable interrupt system	1
HLT	Stop computer operation	1

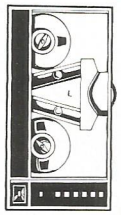
Operation code: 1XXXX

XXXX - Designate the code of the 10 external control instructions, of 4 data channel instructions, and two spare codes.

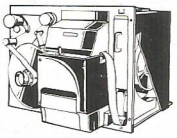
input-output instructions

data channel instructions

Mnemonic	Description	Cycles	Operation Code Format and Notes
ISM	Sequential input to memory; if placed in the memory location related to an interrupt level, performs during interrupt phase, the following operations: — increments the content of a memory location WC (Word Counter); when (WC) = O skips to a location where an end of block service subroutine initiates. Reads the content of location AC (Address Counter) and stores the data from selected device in location addressed by AC which is then incremented	6	For code see external control instructions. The condition (WC) = O is indicated by the status word device. The ISM and OSM instructions can be used in interrupt mode data transfer up to a rate of 120.000 words per second, due to the fact that all arithmetic registers (A, B, X) remain unchanged.
OSM	Sequential output from memory; performs operation inverse of the ISM but in the same mode	6	
ICM	Increments the memory; if placed in the memory location related to an interrupt level, performs during interrupt phase, the following operations: — Adds the data from selected device to the content of a reserved location S and uses the result as actual address for memory increment operation. If the incremented word overflows, skip is provided to a location where an overflow service subroutine initiates.	4	This instruction is particularly valuable in nuclear spectrometry and permits connection, in interrupt mode, of an analog-to-digital converter featuring a counting rate of up to 180.000 counts per second.
ADM	Add to memory; if placed in the memory location related to an interrupt level, performs during interrupt phase, the following operations : — Increments the content of a memory location WC (Word Counter); when WC = O, skips to a location where an end of measurements service subroutine initiates. — Reads the content of location AC (Address Counter) and adds the data from selected device to the contents of location addressed by AC which is then incremented.	7	This instruction is particularly useful for analog signal sampling performed with an analog-to-digital converter connected in interrupt mode, when averaging measurements are required. Sampling rate is up to 100.000 samplings per second.



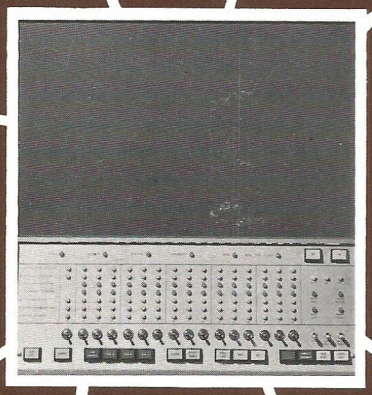
POTTER SC-1030
MAGNETIC TAPE



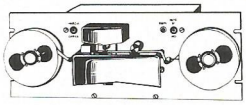
FACIT PE 1500 TAPE PUNCH

TELETYPE ASR-33 or
ASR-35 TELEPRINTER

DISPLAY EQUIPMENT

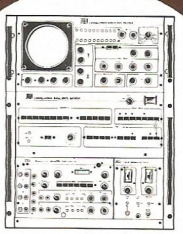


OLIVETTI TE 300
TELEPRINTER



REMEX PUNCHED TAPE READER

LABEN ANALOG-TO-
DIGITAL CONVERTER



LABEN MULTICHANNEL
ANALYZER

input-output

software

The LABEN Computer Division offers a comprehensive software package for the LABEN 70 Digital Processor. Some of the basic programs are listed below. Especially designed programs for specific customer applications can be developed upon request.

monitor

Monitor, the LABEN 70 Operating System, has been designed to enhance inherent system programming and operating efficiency by minimizing storage space and computing time. A prime consideration throughout the design of the system has been maximum use of very small resident program to maintain continuity of job processing and to provide interrupt capabilities for a wide choice of input/output devices.

Additional operation repertoires for utility operations, program debugging, library editing and program loading are stored in the system file and called into storage for execution when needed.

Monitor consists of a modular set of programs designed to operate on all configurations of the LABEN 70 Digital Processor.

Extremely flexible, the system allows maximum usage of the various equipment configurations available.

The minimum equipment necessary for operation of Monitor is the minimum equipment needed for computer utilization : the central processor with 4096 words of core storage and a Teletype or similar system.

A system of this type, without a mass storage device, has the system programs individually loaded by the computer operator upon request of the resident Monitor program.

Full capabilities of the Monitor are realized in mass storage system. In minimum systems the input/output control and interrupt processing capabilities are available to the user.

Some of the Monitor's capabilities enable the user to provide the following operations :
Single job processing
Batch processing
Compile or assemble, load and execute on a mass storage
Loading relocatable programs
Loading absolute programs
Input/output control and interrupt processing
Logical to Physical unit assignments
Library routines
Debugging Aids
Calling and Executing utility and maintenance routines.

fortran

FORTRAN is a formal language with a set of statements, expressions and operators, which are used to simplify the preparation and check-out of computer programs to solve scientific calculation and data handling.

The FORTRAN Compiler produces an object relocatable program, completely compatible with those produced by Assembler. These relocatable programs are linked and loaded by the Monitor's Relocatable Loader.

An ASA FORTRAN IV Compiler can operate on the LABEN 70 Digital Processor with 8 K words of core memory.

assembler and extended assembler

The Assembler allows the programmer to code instructions in a symbolic language (source program) and then translates, in two steps, the source program into object program.

Full Extended Assembler capabilities are available in a system with at least 8192 words of core storage. In a system with 4096 words the Assembler is provided.

Major advantages are :

— Symbolic referencing of storage addresses and instructions
— Storage allocation capability
— Storage reservation
— Convenient data representation
— Relocatable programs: the Assembler can produce object code in either relocatable or absolute format.
— Program linking: ability to link together separately assembled programs at load time
— A FORTRAN compatible COMMON is provided for data communication between subroutines and links
— Defined Macros: a single mnemonic defines a whole series of instructions (call arithmetic and I/O subroutines)
— Program listings: the listing includes the source program, octal location and assembled instructions, error diagnostics and sorted symbol list
— Error checking: all source programs are checked for coding errors.
— IF control: ability to specify with a control statement the sections of the source program to assemble or skip.

mathematical subroutines

The Mathematical Subroutine Library includes routines for logarithmic, exponential, trigonometric and hyperbolic functions, and arithmetic routines for single and double-precision calculations.

debugging aids

Debugging Program is particularly suited to Assembler output, though it can also help in the debugging of object programs from other compilers. Print requests, display of storage areas, dumping at the normal or check termination of a job, linking to utility programs prior and after test execution, are provided.

diagnostics

Emphasis has been placed on the design of a comprehensive library of diagnostic programs. These programs are designed for ease of maintenance.

The following functions are performed:

1. Memory check board test
2. Memory address test
3. Memory parity test
4. Certification of current operation
5. I/O diagnostics.

Diagnostics programs are organized and documented for utilization by technicians with minimum training and experience.

configurations

The basic system configuration is the following:

1. Central processor with 4K memory capable of accomodating up to 8 interface cards (with one or two interface cards for peripheral devices), and power supply. Memory can be extended to 8 K without the need for additional frame or power supply. The basic system is available in the version for standard rack mounting or for accomodation on a bench or housed in an appropriate cabinet (see physical dimensions below).

2. A Teletype ASR 33 or Olivetti TE 300.

The LABEN 70 can be arranged in a variety of configurations to suit possible expansion of the memory from the basic size of 4 to 32 K words, addition of peripheral units selected among the complete range developed for use with the computer, but primarily in relation to the options incorporated in the basic unit and designed to enhance inherent system computing and data processing capabilities.

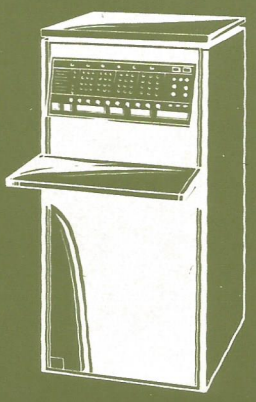
options

— Hardware multiply and divide
— Direct memory access channels
— Memory protect system
— Real time clock
— Power failure protection and restart system.

physical dimensions

Wide : 500 mm.
High : 500 mm.
Deep : 600 mm.

Wide : 560 mm.
High : 1110 mm.
Deep : 650 mm.



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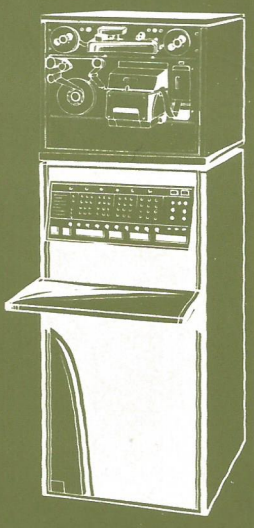


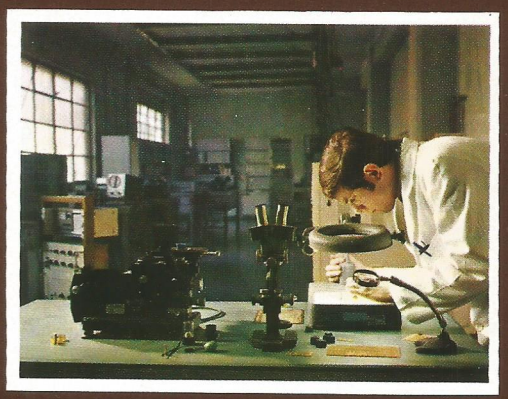
In keeping with its design philosophy, LABEN has developed the LABEN 70 Computer to integrate its range of scientific digital instrumentation with stored-program facilities to provide complete and versatile systems for automatic data processing in all fields in which it has already gained prominence as a leading manufacturer.

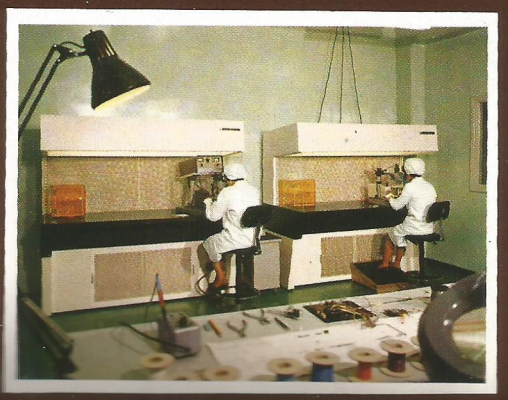
NUCLEAR AND BIOMEDICAL RESEARCH:

- *Multichannel analyzers for nuclear spectrometry*
- *Analog-to-digital converters for connection with analyzers and digital computers*
- *Wired-program computers for correlation function and signal averaging measurements in biomedical, chemical, and engineering applications*
- *Fast counting assemblies for nuclear experiments*
- *Low-noise preamplifiers and linear amplifiers*
- *Germanium - Lithium drifted detectors*

SPACE INSTRUMENTATION

- *PCM telemetry systems for use on board space vehicles (satellites, missiles, aircrafts)*
- *Sequence programmers*
- *Ferrite-core memory units for data storage in space applications*
- *Data compression and digital adaptive telemetry systems*
- *Vibration analyzers for on-board applications*
- *PCM decommutation and display stations*
- *Vehicles check-out stations via PCM telemetries*





INDUSTRIAL SYSTEMS:

- *PCM telecontrol and telemetering systems*
- *Chronological event recorders*
- *Modular data loggers - Digital recorders*