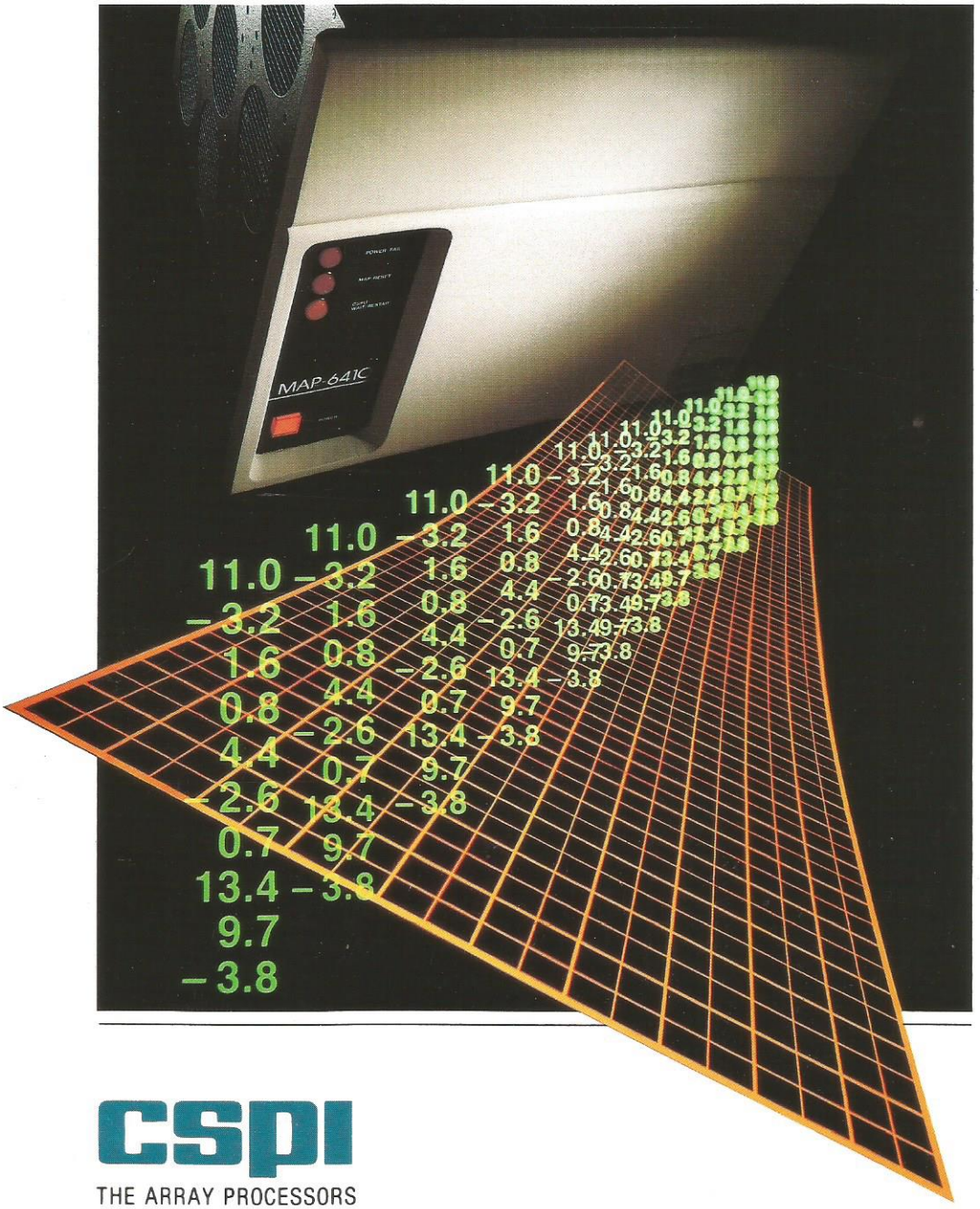
The MAP™-6410 Array Processor



cspi

THE ARRAY PROCESSORS

With MAP-6410, CPSI is setting a new standard of price/performance. MAP-6410 is a 64-bit array processor that provides multi-purpose, multi-precision, high speed calculation at a lower cost than many single precision array processors.

CSPI has been leading the way in array processing with the introduction of MAP array processors in 1975, and the 64-bit MAP-6400 in 1979. Now, CSPI is leading the way to affordable 64-bit array processing with MAP-6410, the powerful and flexible alternative.

MAP-6410...The Affordable 64-bit Array Processor

Powerful. MAP-6410 combines computational precision and speed with impressive software power. Three levels of MAP software provide FORTRAN access to MAP's high performance for a wide range of applications. CSPI's newest software enhancement is the Matrix Accelerator Package (MAXPAK™), which allows any FORTRAN programmer to use the MAP for matrix computations automatically, with no special training in array processing.

Extensive Software:
- MAXPAK
- SNAP-II
- Assembly Language

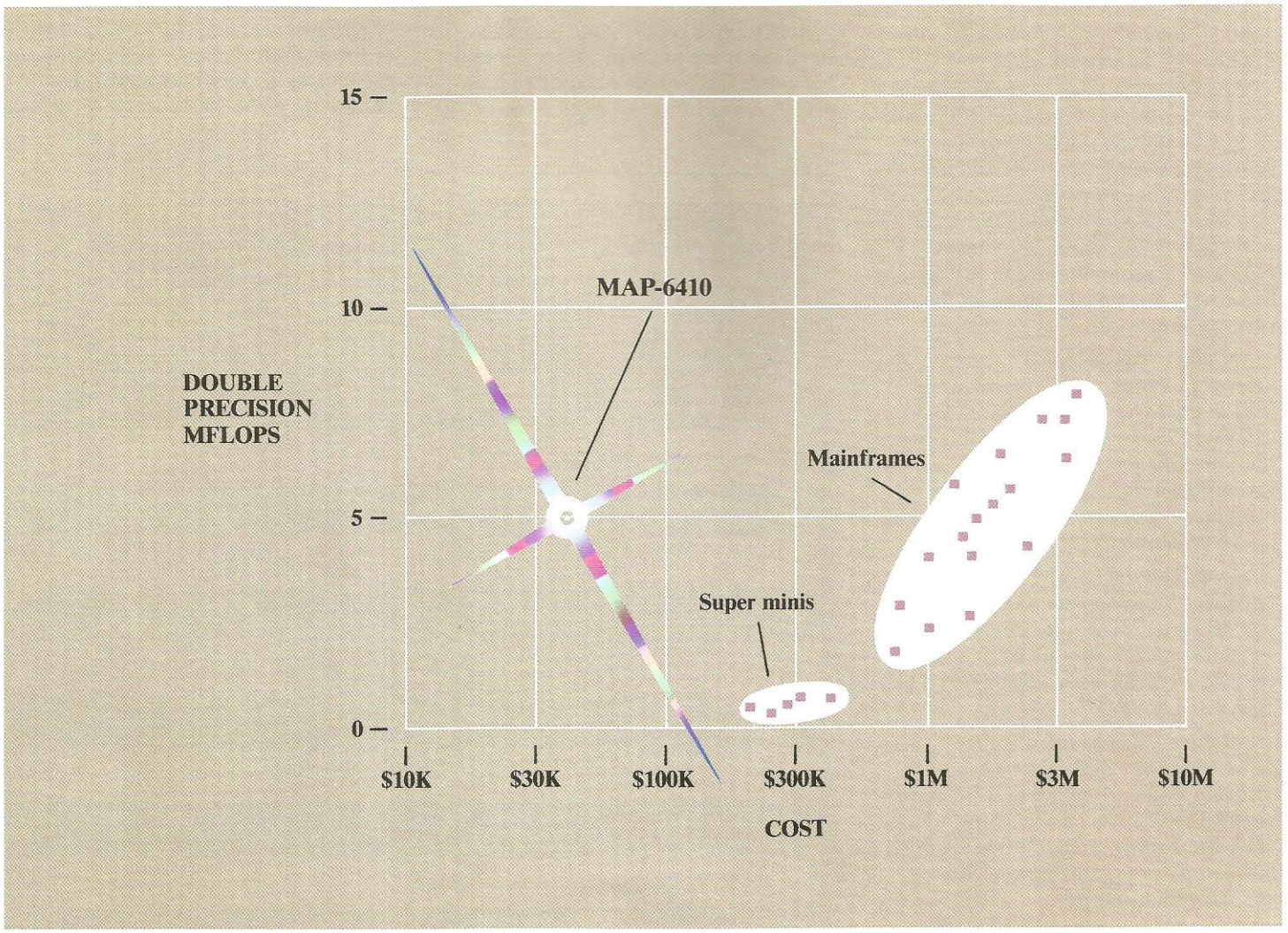
Flexible. For configuration versatility, CSPI has the broadest selection of hardware options available for array processors. Furthermore, a MAP-6410 programmer may choose among data formats ranging from 8-bit fixed-point to 64-bit floating-point. These features, combined with the extensive SNAP-II library, make MAP-6410 as adept at image and signal processing as it is at double-precision numerical computation. Unequaled flexibility makes MAP-6410 the best choice for any computer facility that serves a number of different users and applications.

Applications Versatility:
- Simulation
- Modeling
- Matrix Algebra
- Signal Processing
- Image Processing
- Data Acquisition

Affordable. With reasonable price, size, power, and maintenance requirements, MAP-6410 fits easily into computer facilities and budgets. The modular MAP design is also easy to upgrade, allowing it to follow changes in a user's requirements and protecting it from obsolescence. Moreover, CSPI's aggressive research and development effort in 64-bit array processing will provide new software products and enhanced capabilities for years to come. Existing MAP-6410 systems will be able to grow into these enhancements because of MAP's modularity.

Economy:
- Low power
- Reliable
- Upgradeable
- Inexpensive

Price Performance



Performance Through Advanced Design

Parallel Processing Performance

Although an array processor's speed is delivered through its software, performance originates in its architecture. Since its inception in 1975, the MAP architecture has been widely recognized as the best design at providing not only arithmetic speed, but also the parallel memory, I/O, and control capabilities that are also essential for high throughput.

The MAP architecture is built around a memory bus structure consisting of independent program and data memories. These independent memories avoid many of the memory contention bottlenecks that limit other array processor designs.

The number crunching power of the MAP-6410 is provided by its Arithmetic Processor (AP). The AP performs full 64-bit arithmetic at 5 MFLOPS without pipelining, resulting in more versatile performance than competitive architectures. This is indicated by the function timings shown in the Performance Table.

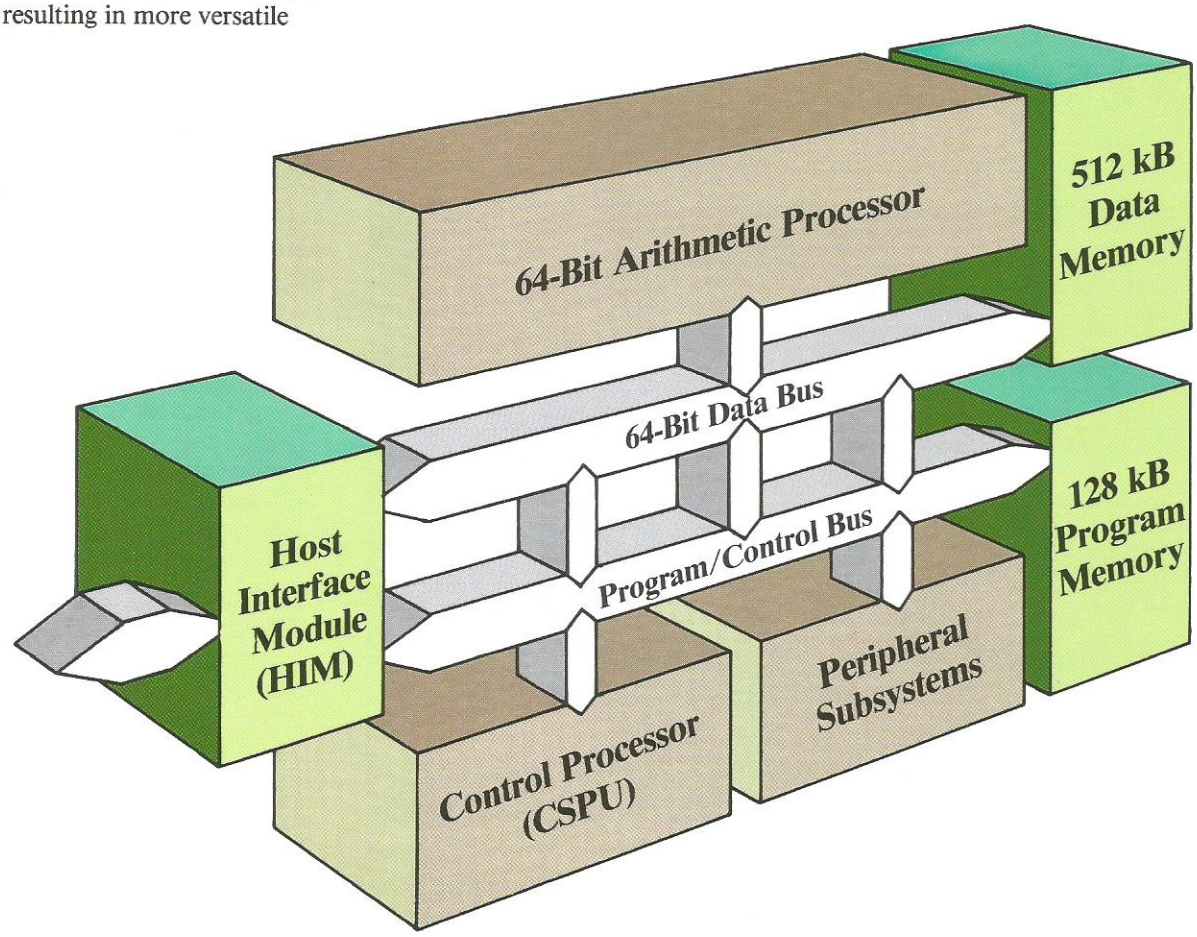
Data transfers can be carried out either through the Host Interface Module (HIM), or through the many types of high-speed peripheral interfaces available on a MAP-6410. A single MAP system may contain up to 8 such DMA interfaces, allowing flexibility in meeting any external storage or real-time data acquisition requirements.

For overall system control, a MAP-6410 contains its own internal minicomputer, the CSPU. The CSPU runs the SNAP-II operating system, providing the supervisor power and interrupt capability that many array processors require from the host. The CSPU not only improves performance but helps further offload the host CPU.

Since the MAP system contains independent processors for floating point control, arithmetic, and I/O, it is capable of supplying all elements of a computational task for host-independent operation. The MAP can thus provide a near stand-alone environment for some applications, especially real-time problems, entirely through FORTRAN-level calls.

MAP-6410 Performance Table

100 × 100 LU Factorization	0.39 sec
100 × 100 Matrix Inverse	1.6 sec
1000-pt. Complex Multiply	3.8 ms
1000-pt. Dot Product	1.2 ms
1000-pt. Square Root	9.8 ms
1024-pt. Real FFT	13.9 ms

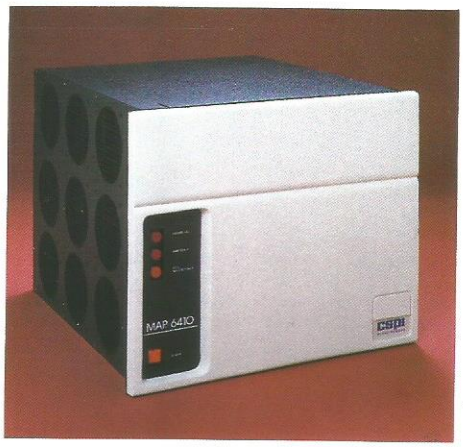


Maintenance and Support

The MAP product line has established an impressive record of reliability, with over 650 installed units averaging over 5000 hours between failures. This is due to CSPI's rigorous manufacture and test procedures as well as the MAP's low component count and power consumption.

To simplify maintenance, the MAP is provided with comprehensive test programs and diagnostics that allow any defective component to be located quickly. Repairs are usually simple board swaps. CSPI offers several maintenance options to cover repairs, exchanges, spares, and training.

CSPI also conducts frequent training courses in FORTRAN-level SNAP-II programming, assembly language programming, SNAP-II Operating System internals, and MAP maintenance. These courses are given either at our Billerica, Mass., facility or at customer sites. Our applications department is available to provide special software development and consulting. Finally, CSPI publishes a bi-monthly MAP newsletter, and MAPUS, an autonomous MAP users group, holds annual meetings to exchange software, advice, and ideas for applications programming.



Specifications

Internal Floating-point Format	64 bits (56-bit mantissa)
Floating-point Multiply Time	880 ns
Floating-point Add Time	270 ns
Number of 64-bit Registers	
Multiplier	14
Adder	14
Internal Data Stack	1024
AP Program Caches	
Arithmetic Instructions	4096
Addresser Instructions	256
Memory Specifications	
Program Memory	128 KB
Data Memory	512 KB
Memory Access Time	500 ns
64, 32, 16, or 8 bit addressability	

I/O Processors (up to 8 per system)
- Analog Data Acquisition Module (up to 16 channels)
- Analog Output Module (2 channels)
- I/O Scroll 2 (up to 8 MB/sec.)
- I/O Scroll 4 (up to 36 MB/sec.)
- Disk Interface Subsystem
- Bulk Memory Interface Subsystem

Host Interfaces

Consult CSPI for an up-to-date list of supported host computers and operating systems

Worldwide Sales and Service

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