PDP-9


PDP-9
DIGITAL EQUIPMENT CORPORATION/MAYNARD, MASSACHUSETTS
PRGM STOP
INSTRUCTION
PC
PS REGISTER
TRAP
EXD
CLK
SING STEP
SING INST
REPT
PARITY ERROR
START
PROGRAM STOP
CONTINUE
EXAMINE
EXAMINE NEXT
DEPOSIT
DEPOSIT NEXT
I/O RESET

PDP-9 ... the big one in the low price field

The big features of the PDP-9 provide greater processing power than any other computer in its price class. The PDP-9's 18 bit word length provides greater accuracy per word and simpler programming than the smaller word length machines. A PDP-9 18 bit word can directly and simply address a full 8192 word memory module. The hardware is there to do on-line control, data reduction and computation without round-about programming. PDP-9 modular software expands to use the machine fully.

Starting with the basic PDP-9, the researcher or systems designer can have full system power without add-on's. When he wishes his system to grow, the PDP-9 has both the standard options and modular software to do it.

PDP-9 BEGINS BIG

The basic PDP-9 computer system has an 8,192 word ferrite core memory, bi-directional input/output bus, direct memory access channel (with true cycle stealing), and four high speed data channels. The 18 bit word can have an optional parity bit. There is a high speed control memory, a high speed adder and a real-time clock. The basic PDP-9 also has a 300 character-per-second paper tape reader, a 50 character per second paper tape punch and input/output teleprinter. All 8,192 words are directly addressable. I/O transfer rate up to 18,000,000 bits per second; add time is two microseconds. Hardware and software are ready now. All this in the low price field.

PDP-9 EXPANDS BIG

The basic PDP-9 expands with powerful central processor options, 8,192 word memory modules and a wide variety of input/output options. Core memory expands up to 32,768 words. Bulk storage devices include low cost DECtape and IBM compatible magnetic tape. Input/output devices, such as DEC's own A/D converters and CRT displays, may either be attached to the I/O bus and use programmed or data channel transfers or be interfaced to the direct memory access bus for one-cycle, true cycle-stealing, direct transfers to memory. Configurations are easily tailored with standard options. Special devices are easily and economically interfaced with standard FLIP CHIP™ circuit modules.

To take full advantage of the expanded PDP-9 systems, the PDP-9 has a modular device-independent software package.

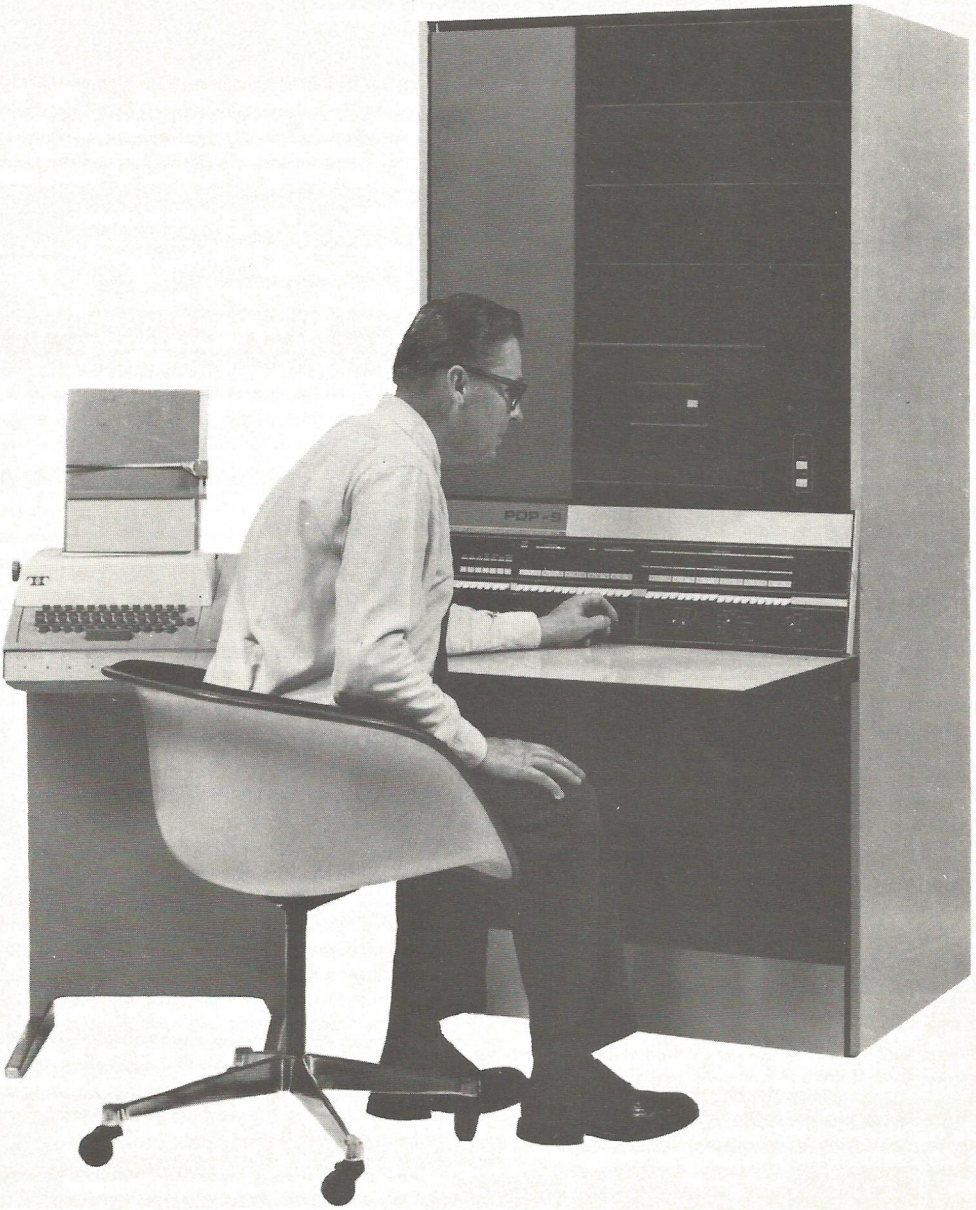
BIG PDP-9 SOFTWARE

PDP-9 basic software is completely compatible with software available on the popular PDP-7. The PDP-9 Extended Software Package makes full use of expanded PDP-9 configurations. New software includes real-time FORTRAN IV, a versatile macro assembler, a control monitor, a 6 and 9 digit floating point arithmetic package, an on-line editor, an on-line debugging system, and a modular I/O programming system that eliminates the need to program standard peripheral devices.

BIG BACKGROUND IN RESEARCH AND ENGINEERING

The PDP-9 is a direct lineal descendant of the PDP-1, PDP-4, and PDP-7. DEC's 18 bit word computers have established an important community that share programs and techniques through one of the most effective user's groups in the computer field.

Over a thousand DEC computers are being used in on-line research and engineering alone. DEC's background of experience in your field results in one of your most important assets: the DEC field engineer. He is prepared to discuss your requirements in light of hundreds of the on-line data taking and control problems similar to your own. He has applications literature and the names of others using computers in your field; his phone number is listed on the back cover of this brochure.


PDP-9

BIG PDP-9 CENTRAL PROCESSOR

Figure 3 illustrates the basic organization of the PDP-9 central processor. Using a transfer bus system, data is transferred between registers with DC levels to minimize timing problems (level logic is used in the central processor). All active registers use simple circuit designs, there are no logical delays.

FEATURES

Control Memory — The Control Memory is a very fast read-only, prewired magnetic core storage unit. It stores all sequences of internal micro-instructions required to fetch and execute a program's instructions, to effect operation of the data channels, and to respond to operator commands initiated at the control console.

High Speed Adder — The 19-bit Adder functions as a fast adder-subtractor for arithmetic operations, and as the transfer path for all inter-register transfers and shift operations. It can add two 19-bit words in 200 nanoseconds.

Real-time Clock — The Real-time Clock generates a pulse every 16.7 milliseconds for 60-cycle systems (every 20.0 milliseconds for 50-cycle) and automatically increments location 00007. It may be used as either an elapsed time counter or an interval timer. When overflow of location 00007 occurs, the clock requests a program interrupt which can be used to transfer control to a subroutine.

Convenient Control Console — The Control Console (or operator's console) contains the keys, switches, and lights required for operator initiation, control, and monitoring of programs. Some of the features of this console are:

- A read-in switch to initiate the reading of paper tapes
- Single-step and single-instruction switches
- REGISTER indicators and REGISTER DISPLAY switch that allow continual monitoring of key points in the system such as the accumulator, arithmetic register, memory quotient, program counter, input/output bus, paper tape reader buffer, paper tape punch buffer, teletype buffer, and input/output status flags
- EXAMINE and EXAMINE NEXT switches that allow the manual examination of the contents of any memory location
- 18-switch register for manual entry of data and instructions or sense-switch capabilities

ELEMENTS

Accumulator — The PDP-9 Accumulator, an 18-bit register, retains the results of arithmetic/logical operations for the interim between instructions.

Link — A one-bit register, the link acts as an extension of the Accumulator. Its contents may be program sampled and program modified.

Arithmetic Register — The Arithmetic Register functions with the Accumulator to perform arithmetic and logical operations.

Timing Control — The Timing Control generates clock signals governing the timing of internal processor operations and the synchronization of core memory and input/output devices to these operations.

Control Register — The Control Register delivers control signals to the transfer busses and to the active registers.

Multiplier-Quotient Register — The optional Extended Arithmetic Element adds the 18-bit Memory Quotient Register to the basic PDP-9 for double-precision products in multiplication and dividends in division.

Program Counter — The Program Counter retains the address of the next instruction to be executed.

Instruction Register — The Instruction Register accepts the instruction code of each word fetched from memory and supplies it to the Control Memory.

Memory Buffer Register — The Memory Buffer Register is the interface for information transfers between the processor and memory.

PDP-9 CENTRAL PROCESSOR OPTIONS

Extended Arithmetic Element — The Extended Arithmetic Element adds high-speed multiply, divide, normalize, and shifting instructions to the basic PDP-9. Typical operation times (depending on number of steps specified) are:

Multiply — 3 to 11 microseconds

Divide — 3 to 11 microseconds

Normalize — 2 to 17 microseconds

Shift — 2 to 17 microseconds

Memory Extension Control — Memory Extension Control, a prewired PDP-9 option, extends PDP-9 addressing capability to permit addition of up to three additional 8,192-word core memory modules, for a system total of 32,768 words.

Power Failure Protection — With the power failure protection option added, PDP-9 is not affected by line power interrupts of less than 25 milliseconds duration. An interrupt of greater duration initiates a program interrupt in which a subroutine can save the contents of active registers (Accumulator, Multiplier-Quotient, Program Counter, Link). A restart provision allows automatic program resumption following the return of line power.

BIG PDP-9 CORE MEMORY

The PDP-9 core memory uses a new 2½D flat pack design concept and operates with a cycle time of 1.0 microsecond; add time is 2.0 microseconds.

Each 8,192-word core memory module contains a core stack, sense amplifiers, drivers, and a memory address register. The latter sets up the memory location (address) to be used for data retrieval or storage.

System core memory can be expanded from the basic 8,192 words up to 32,768 words in 8,192-word increments. Such expansion requires the memory extension control to extend PDP-9's addressing capability.

Direct Memory Access Channel

Each PDP-9 memory module has a two-port capability for data entry and retrieval. One port, connecting to the memory bus, services the processor. The other allows direct and immediate access of memory by a peripheral device for fast data transfers via a direct memory access bus. A device request for direct memory access service has priority over a processor or program request.

Parity Option

Parity checking may be optionally added to each memory module (word length is increased to 19 bits). A control on the processor console allows the program to be stopped upon detection of a parity error at the programmer's option.

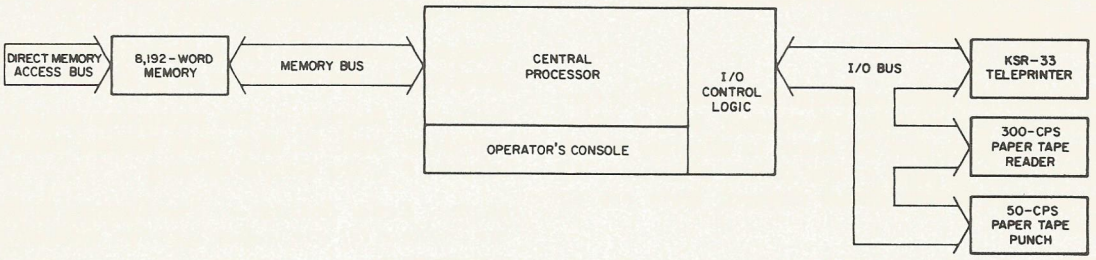


Figure 1 Basic PDP-9

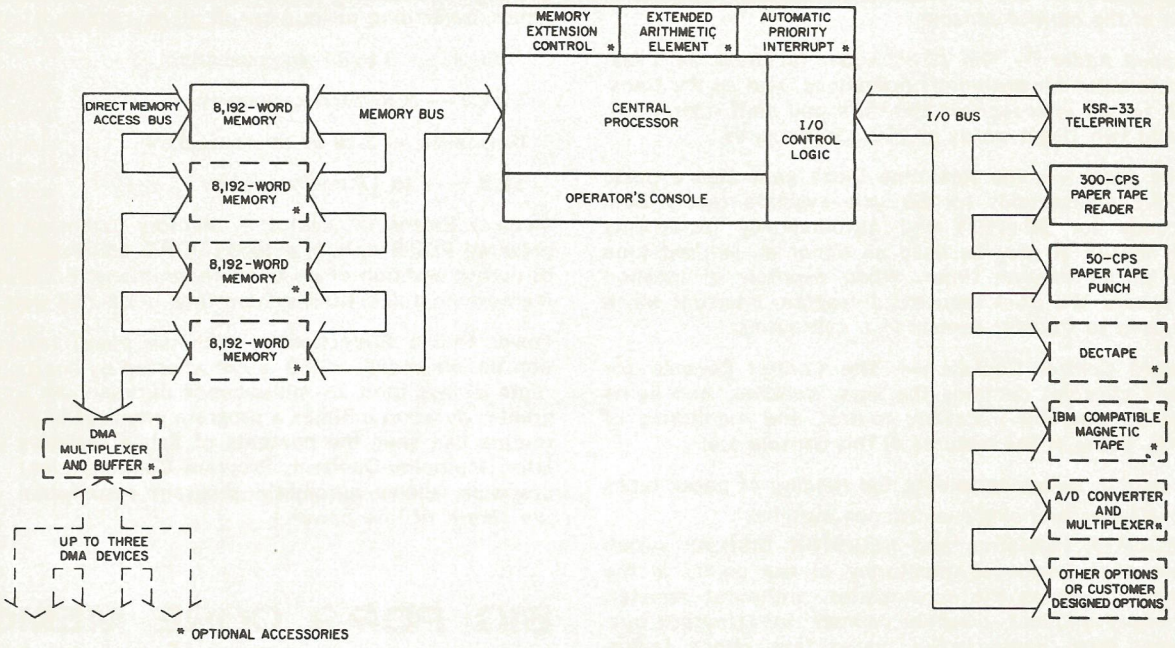


Figure 2 Expanded System Configuration

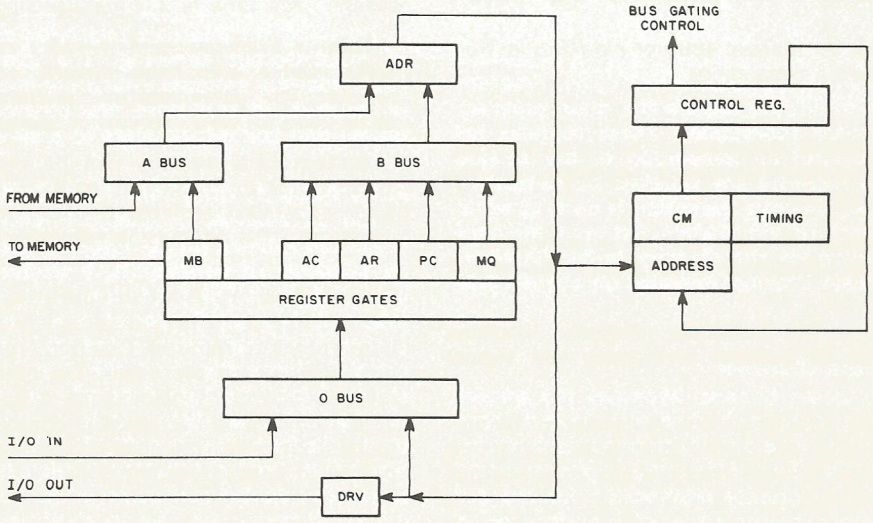


Figure 3 Central Processor Organization

BIG INPUT/OUTPUT FACILITIES

PDP-9 Input/Output devices may be attached to either the bidirectional Input/Output Bus or the Direct Memory Access Channel. The Input/Output Bus can be used for all programmed transfers and data channel transfers, while the Direct Memory Access Channel is used for extremely fast (50,000-1,000,000 wps) devices that must have immediate access to memory.

Input/Output Bus

The Input/Output Bus is a set of data and control lines that serially link peripheral device controls to the central processor. It can select any one of sixty-four (64) devices, and up to four (4) sub-devices within any device. Up to three (3) Input/Output pulses can be issued to any device, so that (64 x 4 x 3 =) 768 different Input/Output commands are available on the bus.

Data Transfers

Input/Output data transfers function within the following priority structure.

1. Direct Memory Access Channel requests (highest priority)
2. Data Channel requests
3. Priority interrupts (8 levels) — optional
4. Program interrupts
5. Main program

A higher priority request for service interrupts any in-process service of a lower priority at the end of the current instruction, or, in the case of the Direct Memory Access Channel, at the end of the current memory cycle. Program interrupts and priority interrupts require the main program transfer control to service subroutines. These routines restore the program's control at completion of the service interval. Data Channel requests are satisfied by computer-granted data breaks; i.e., program execution is delayed while the Data Channel transfers information between memory and the requesting device via the Memory Buffer Register. The Direct Memory Access Channel operates on a true cycle stealing basis.

Direct Memory Access Channel

The Direct Memory Access Channel bypasses the central processor to provide a data path between system core memory and high-speed peripherals. Up to three devices can be concurrently serviced by the addition of an optional multiplexer which establishes a priority relationship for the devices. The Direct Memory Access Channel functions on a "cycle stealing" basis; i.e., a device request for service defers execution of the main program for one memory cycle, during which time a word is transferred to or from core memory. Program execution resumes upon completion of the transfer cycle. The Direct Memory Access Channel accesses memory through its own entry port to each memory module.

Data Channels

Data Channel operations use the Input/Output Bus for data transfers between core memory and high data rate peripherals (DECtape, magnetic tape, etc.). The Data Channel facility will concurrently service up to four devices and can be expanded to eight devices; priority is established at the hardware interface.

The channels function with processor-granted data breaks to interleave transfers with execution of the program in progress. Data is read into memory in three cycles and out of memory in four cycles.

Program Controlled Transfers

Program controlled transfers are made by Input/Output Transfer (IOT) instructions contained in the main program or in service subroutines. These instructions are microcoded to effect response only for a particular device. The microcoding includes issuing of a unique device selection code and appropriate processor-generated pulses to initiate the specified operation.

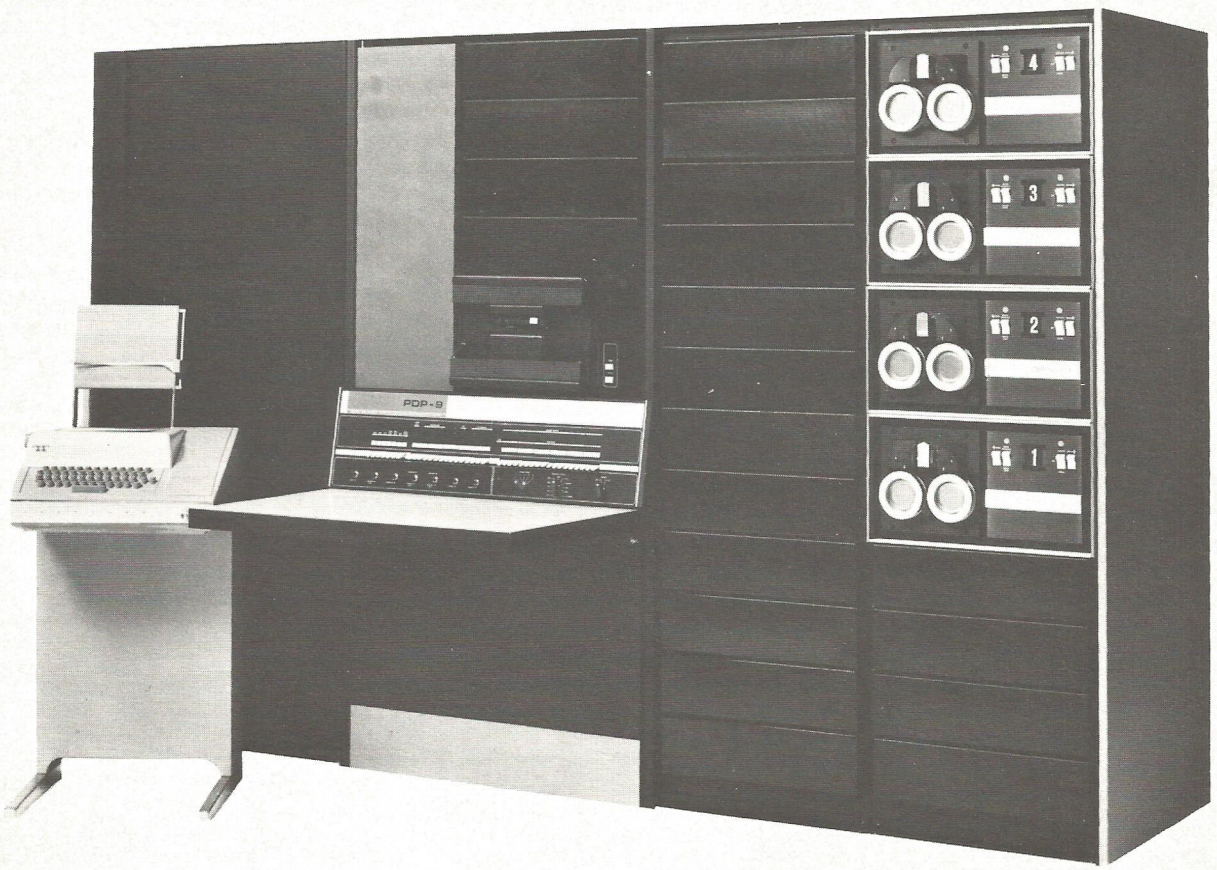
For an "out" transfer, the program reads a data word from memory and places it on the Input/Output Bus. A subsequent Input/Output Transfer instruction selects the device and causes it to enter the word in its data buffer register. For an 'in" transfer, the process reverses. An Input/Output Transfer instruction selects the device and causes the contents of its data buffer to be gated onto the Input/Output Bus. In turn, the word is strobed into the accumulator and stored, by the program, in memory.

Program Interrupt

The program interrupt facility offers an efficient method of Input/Output servicing. The computer continues with execution of a program until a peripheral signals that service is required. At that time, the program in process is interrupted and control transfers to a service subroutine.

Automatic Priority Interrupt Option

The 32 channel Automatic Priority Interrupt system extends the PDP-9's Input/Output capabilities to include priority servicing of peripherals, a useful feature for programs operating in real-time environments. The Automatic Priority Interrupt has eight ranged levels of priority; each takes precedence over lower automatic priority interrupt levels, program interrupts, and the main program. This priority structure permits high data rate or critical devices to interrupt servicing of slower or less critical devices with minimum program "overhead". The four higher levels are for fast access to Input/Output service subroutines in response to device-initiated service requests. Each of these levels permit multiplexing, i.e., up to eight devices may be assigned equal priority. The four lower automatic priority interrupt levels are assigned to the processor. Activity on them is limited to program-initiated requests for transferring control to programs or subroutines on a priority basis.


PDP-8
4
3
2
1

BIG PERIPHERAL OPTIONS

Mass Storage Devices

DECtape Control Type TC02 and Transport TYPE TU55

The DECtape system provides a unique fixed-address magnetic tape facility for program and data storage. The DECtape Control transfers direct to memory via the Data Channel facility and can handle up to eight transports. Each transport stores 3,000,000 bits of information at 375 bpi and 80 ips.

Magnetic Tape Control Type TC59 and Transport Type 545

The Automatic Magnetic Tape Control transfers data to and from IBM-compatible magnetic tape transports via the Data Channel facility. Each control can handle up to eight transports and can read or write in BCD or binary modes. The Type 545 transport can handle 7-channel tapes at 200,556, and 800 bpi and 45 ips. A 75 ips transport will also be offered.

Magnetic Drum System Type RM09

Operates through the Direct Memory Access Channel for true cycle-stealing access to memory. Available in 32,768-word, 65,536-word, and 131,072-word sizes.

Display Systems and Accessories

Precision CRT Display Type 30D

Plots data point by point on a 16-inch cathode ray tube in a raster 9⅜ inches square having 1024 points on a side. Separately variable 10-bit X and Y coordinates. Includes program intensity control. Plotting rate is 35 microseconds per point.

Oscilloscope Display Type 34H

Controls the plotting of data point by point on an X-Y plotting scope such as the Tektronix Model RM 503. Raster size is 1024 x 1024 points.

Programmed Buffered Display Type 339

Interfaces to PDP-9 to provide up to 1400 inches of vector (20,000 points) or 1200 characters flicker free on 9⅜-inch square raster. System includes DMA Multiplexer Adapter, High Speed Light Pen, and push-button function box. Character generator, zoom option, search option, and slave mode available as extras.

Precision Incremental CRT Display Type 340

Plots points, lines, vectors, and characters on a 1024 x 1024 raster 9⅜ inches square. Plotting rate is 1½ microseconds per point in vector, increment, and character modes, while random point plotting takes 35 microseconds. Interfaces to Direct Memory Access Channel via DMA Multiplexer Adapter.

High Speed Light Pen Type 370

Uses fiber optic light pipe and photomultiplier system for fast detection and modification of information displayed on the precision CRT display.

Card Input Equipment

Card Reader and Control Type CR01E

Reads standard 80-column cards at 100 cpm. Bin capacity for 430 cards.

Card Reader and Control Type CR02B

Reads standard 80-column cards at 200 cpm in binary or alphanumeric modes.

Line Printers and Plotters

Line Printer and Control Type 647

Prints 120 columns, 64 characters per column. Available at 300 and 600 lines per minute. Includes 120-character buffer.

Incremental Plotter and Control Type 350

Performs high resolution plotting on paper 12 or 31 inches wide at rates of 12,000 or 18,000 points per minute. Plotting increments are 0.005 and 0.01 inch.

Data Communications Systems

Multiple Teletype System Type LT09

Provides inexpensive interface to PDP-9 for up to five teletypes (KSR-33, ASR-33, KSR-35, or ASR-35). Several LT09 units may be attached to the PDP-9.

Data Communications System Type 680

Provides high-capacity data communications system without tying up PDP-9 central processor. Includes PDP-8 in Type 680 system, interfaced to PDP-9 via Interprocessor Buffer, Type DB98A. Can handle up to 128 teletype stations.

Analog-to-Digital Converters

General Purpose Analog-to-Digital Converter Type 138E

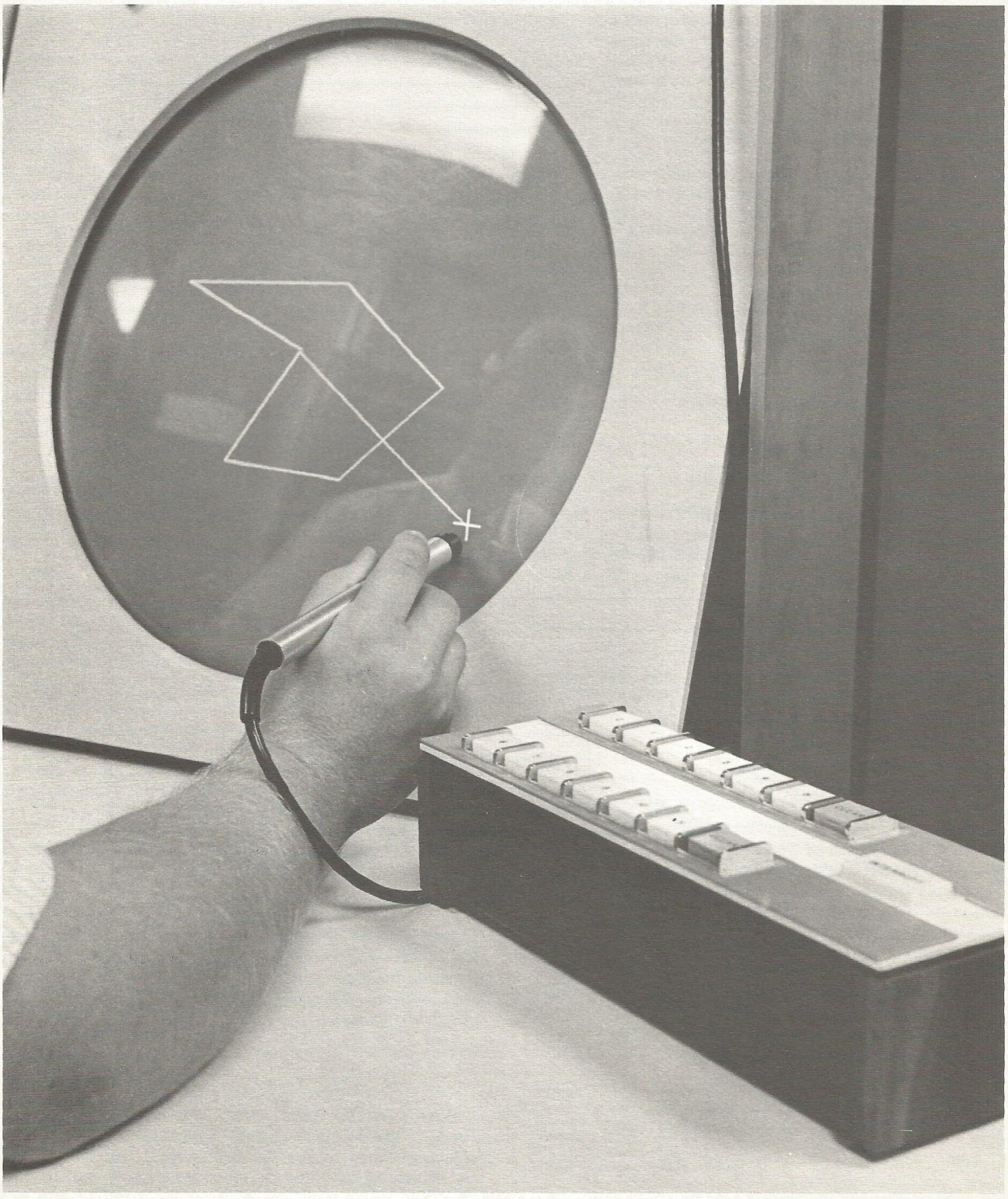
The Type 138E is a high-speed, successive approximation converter with switch-selected word length from 6 to 12 bits and switch-selected error from ±0.8% to ±0.025%. Conversion time varies from 9 to 35 microseconds according to these switch settings. Analog input signal range is 0 to −10 volts.

General Purpose Multiplexer and Control Type 139E

Up to 64 analog input channels can be selected for application to the input of the Type 138E by the Type 139E. Channels can be program selected in sequence or by individual address. The number of channels that can be selected is determined by the number of optional Multiplexer Switches Type A100 used in the Type 139E. Each Type A100 can select two channels.

Digital-To-Analog Converter Type AA01A

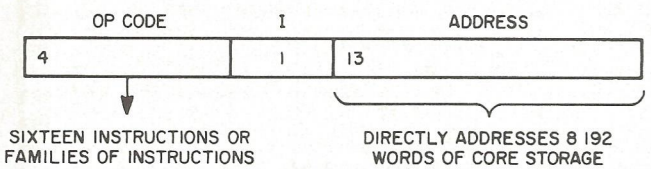
The Type AA01A D/A converter is used to convert 12-bit binary numbers to analog voltages. There are three separate converters and three digital buffer registers in each AA01A. Register updating is accomplished through one 12-bit input channel.



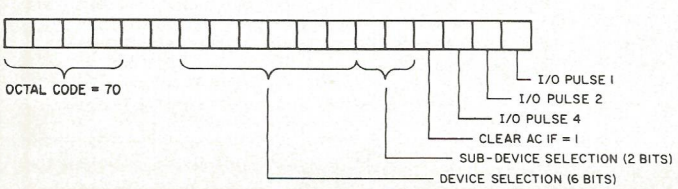
BIG PDP-9 INSTRUCTION REPERTOIRE

PDP-9 Order Code

The PDP-9 eighteen-bit word is decoded as shown below:



Of the 16 instruction codes available, 13 are memory-reference instructions and use the format shown above. Of the other three, one provides for the "Operate" group of micro-programmed instructions that includes CLEAR ACCUMULATOR, SKIP ON POSITIVE, SKIP ON NEGATIVE, CLEAR LINK, ROTATE, etc. Another provides for the family of instructions that control the optional Extended Arithmetic Element and adds MULTIPLY, DIVIDE, LONG SHIFT, and NORMALIZE instructions to the basic set. The last operation code provides the family of input-output (IOT) instructions which can handle up to 256 devices, with up to three separate pulses per device. The IOT instructions can be micro-programmed to clear the accumulator and issue one, two, or three pulses per word. An IOT instruction format is shown below.



Addressing Modes

Memory reference instructions can use direct or indirect addressing. When a PDP-9 system contains more than 8,192 words of core storage, the Extend Mode is used to address the additional memory banks.

Direct Addressing — 8,192 words of any one memory module in the system can be directly addressed. Locations not in the current 8,192-word memory block are accessed by indirect addressing operation of the memory extension control option.

Indirect Addressing — When indirect addressing is indicated, the addressed memory location is taken as not containing the operand, but the address at which the operand is located. Only one level of indirect addressing is permitted. When in Extend Mode, 15 bits of the indirect word are used as the address, permitting all 32,768 possible words to be accessed.

Extend Mode Addressing — With extend mode, locations not in the same 8,192-word core memory block can be accessed by indirect addressing. Bits 3 and 4 of the indirect word indicate the block in which a location addressed by bits 5-17 resides.

Auto-Index Registers

Eight locations (10_8-17_8) of the 8,192-word module included in the standard PDP-9 configuration act as auto-index registers. When indirectly addressed, the contents of an auto-index register are incremented by one and then taken as the effective address of an instruction. When directly addressed, these locations act like all other memory locations.

INSTRUCTIONS

MEMORY REFERENCE INSTRUCTIONS

MNEMONIC	OPERATION
CAL Y	call subroutine. Y is ignored jms 20 if bit 4 = 0, jms i 20 if bit 4 = 1.
DAC Y	deposit AC. C(AC) => C(Y)
JMS Y	jump to subroutine. C(PC) => C($Y_{5\ 17}$), C(L) => C(Y_0), Y + 1 => C(PC)
DZM Y	deposit zero in memory. 0 => C(Y)
LAC Y	load AC. C(Y) => C(AC)
XOR Y	exclusive OR. C(AC) V C(Y) => C(AC)
ADD Y	add (1's complement). C(AC) + C(Y) => C(AC)
TAD Y	2's complement add. C(AC) + C(Y) => C(AC)
XCT Y	execute.
ISZ Y	index and skip if 0. C(Y) + 1 => C(Y), if C(Y) + 1 = 0, then C(PC) + 1 => C(PC)
AND Y	AND. C(AC) C(Y) => C(AC)
SAD Y	skip if AC and Y differ. If C(AC) ≠ C(Y), then C(PC) + 1 => C(PC)
JMP Y	jump. Y => C(PC)

OPERATE INSTRUCTIONS

MNEMONIC	OPERATION
OPR	operate
NOP	no operation
CMA	complement, C(AC) => C(AC)
CML	complement link, C(L) => C(L)
OAS	inclusive OR AC switches C(ACS) V C(AC) => C(AC)
LAS	load AC from switches C(ACS) => C(AC)
RAL	rotate AC + link left one place C(AC_J) => C($AC_{J\ 1}$), C(L) => C(AC_{17}), C(AC_0) => C(L)
RCL	clear link, then ral. 0 => C(L), then ral
RTL	rotate AC left twice. Same as two ral instructions
RAR	rotate AC + link right one place. C(AC_J) => C($AC_{J\ 1}$), C(L) => C(AC_0), C(AC_{17}) => C(L)
RCR	clear link, then rar. 0 => C(L), then rar
RTR	rotate AC right twice. Same as two rar instructions
HLT	halt. 0 => RUN
SZA	skip on zero AC. Skip if C(AC) = positive zero
SNA	skip on non-zero AC. Skip if C(AC) ≠ positive zero
SPA	skip on positive AC. Skip if C(AC_0) = 0
SMA	skip on negative AC. Skip if C(AC_0) = 1
SZL	skip on zero link. Skip if C(L) = 0
SNL	skip on non-zero link. Skip if C(L) = 1
SKP	skip, unconditional. Always skip
CLL	clear link. 0 => C(L)
STL	set the link. 1 => L
CLA	clear AC. 0 => C(AC)
CLC	clear and complement AC. −0 => C(AC)
GLK	get link. 0 => C(AC), C(L) => C(AC_{17})
LAW N	load AC with law N, where N equals a constant. law N => C(AC)

EAE INSTRUCTIONS

MNEMONIC	OPERATION
EAE	basis EAE command — no operation
LRS	long right shift
LRSS	long right shift, signed
LLS	long left shift
LLSS	long left shift, signed
ALS	accumulator left shift
ALSS	accumulator left shift, signed
NORM	normalize: max. shift is 44
NORMS	normalize, signed
MUL	multiply unsigned
MULS	multiply signed
DIV	divide C(AC and MQ) as a 36-bit unsigned number
DIVS	divide C(AC and MQ) as a 34-bit 1's complement signed number
IDIV	integer divide unsigned
IDIVS	integer divide, signed
FRDIV	fraction divide unsigned
FRDIVS	fraction divide, signed
LACQ	replace the C(AC) with the C(MQ)
LACS	replace the C(AC) with the C(SC)
CLQ	clear MQ
ABS	place absolute value of AC in the AC
GSM	place AC sign in link and take absolute value of AC
OSC	inclusive OR the SC into the AC
OMQ	inclusive OR AC with MQ and place results in AC
CMQ	complement the MQ

IOT INSTRUCTIONS

MNEMONIC	OPERATION
	Program Interrupt
IOF	turn off interrupt
ION	turn on interrupt
ITON	turn on trap, also turns on program interrupt
	IO Equipment
IORS	read status of io equipment
	Clock
CLSF	skip if clock flag is 1
CLOF	turn off clock, clear clock flag
CLON	turn on clock, clear clock flag
	Paper Tape Reader
RSF	skip if reader flag is a 1
RSA	select reader for alphanumeric, clear reader flag
RSB	select reader for binary, clear reader flag
RRB	read the reader buffer into AC, clear reader flag
	Paper Tape Punch
PSF	skip if punch flag is a 1
PLS	punch a line in alphanumeric mode
PCF	clear punch flag
PSB	punch a line in binary mode
	Keyboard Input from Teleprinter
KSF	skip if keyboard flag is a 1
KRB	read the keyboard buffer into the AC, clear keyboard flag
	Teleprinter
TSF	skip if teleprinter flag is a 1
TLS	load teleprinter buffer and select, clear teleprinter flag
TCF	clear the teleprinter flag

BIG PDP-9 SOFTWARE

Software Design Philosophy

Two complete software systems and a maintenance system are available with PDP-9 systems. All three have been designed to meet the following requirements:

Modularity — so that all hardware options present on a system may be utilized.

Sophistocated techniques — to supply the power and versatility required by experienced programmers with complex applications and systems.

Ease of use — so that they are readily understandable and usable by the programming novice. For many applications PDP-9 software will allow problems to be solved the day the computer is delivered.

Basic Software Package

The PDP-9 Basic Software Package provides powerful single-job capabilities to the user of a basic system. Using the basic PDP-9 with an 8,192 word memory, paper tape reader, punch, and teletype, the Basic Software Package is compatible with software available for the current PDP-7.

This system includes both FORTRAN II and IV compilers, an assembler, input-output routines, arithmetic packages, a symbolic tape editor and a debugging system. All input and output for the Basic Software Package is paper-tape-oriented.

Extended Programming System

The extended programming system consists of an executive (monitor) program, an input/output programming system, and the following programming aids: a FORTRAN IV compiler (exceeds ASA standard), a macro assembler, peripheral interchange program, editor, debugging (DDT) program, and relocatable loader. This system affords the most efficient use of peripherals and allows automatic updating of programs to employ standard peripherals added in the future. Additional characteristics are:

1. Rapid, efficient retrieval of any system or user program from the system library.
2. Use of the standard system programs in such a manner that they can accept source data from an output data to any peripheral device.
3. Automatic linkages to correct peripheral equipment at the time a program is loaded.
4. Completely written and debugged input/output routines for use of any peripheral equipment from the most basic device handling level to the more sophisticated device independent subroutine. Automatic buffer handling and code conversion is included when desired. The package completely obsoletes the need for the programmer to concern himself with the peculiarities of specific I/O equipment and allows him to concentrate on the more functional portions of his program.
5. All programs and subroutines are relocatable and make most efficient use of the automatic priority interrupt, extended memory, and extended arithmetic element options.
6. Minimal resident memory requirements.
7. Consistency of control information and internal character code between programs.
8. Minimal specification of control information required.
9. Automatic return to the monitor system.

Descriptions of the major components follow.

I/O Programming System (IOPS)

IOPS provides a standardized programming interface to all I/O devices attached to the PDP-9 system. Symbolic input/output unit assignments allow user programs to select I/O devices specified symbolically to the macro assembler or the FORTRAN IV compiler. IOPS consists of a modular collection of relocatable input/output and utility subroutines which transmit data to and from peripheral devices and make the data readily available for processing. IOPS will be coded on the data and file handling levels to provide device independence for all systems programs.

Specifically, IOPS provides the user with three levels of I/O programs.

1. Device Handling — Providing the basic subroutines to allow the user to operate a device, doing code conversion where required.
2. Data Handling — Providing the data buffering and internal line and character transmission facilities.
3. File Handling — Providing for the manipulation of named files on the system level.

IOPS completely eliminates the need for the programmer to program the standard peripheral devices. The programmer is no longer concerned with input/output problems such as timing, overlap, and differences in the characteristics of peripheral devices. This permits him to concentrate on his primary task — the processing of data inside the computer.

IOPS is coded on a modular basis to allow addition of new devices and modifications to the handling of current devices. It requires considerably less effort to modify an IOPS subprogram than to revise individual input/output sections to fit a new configuration. If IOPS is used, programs can be changed more rapidly to fit the expanded configuration.

FORTRAN IV Compiler

The FORTRAN IV compiler translates source programs into object programs acceptable to the linking loader. Comprehensive source language diagnostics are output by the compiler if language errors exist in the source program. It operates in the interrupt mode during compilation so that information is immediately available to the processor alleviating the need to wait for peripheral devices. In addition, it generates an object program capable of transferring data from peripherals via the interrupt, buffering it, and making it immediately available to the program. Lastly, the compiler reads source programs from any input unit and writes listings and object programs on any output unit.

The operating system performs input/output and arithmetic functions as directed by the object program at runtime. The real-time capabilities of the operating system include the ability to control buffering and the ability to directly communicate with IOPS interrupt service subroutines.

Macro-9 Assembler

Macro-9 is a two-pass assembler offering facilities beyond the PDP-9 symbolic assembler.

The Macro-9 assembler accepts programs written in the PDP-9 symbolic assembler language, and allows use of nested, recursive, and self-redefining macro and conditional assembly.

Relocatable Linking Loader

The linking loader can load any Macro-9 or FORTRAN IV object program from any input device, set up symbol tables for debugging, load programs into extended memory, automatically load and link system subroutines (including IOPS) from the system library.

Conditional loading of separately relocatable segments within one source program is available to allow loading only those functional elements or parameters of a subroutine actually required.

Maintenance and Diagnostic Programs

With the PDP-9, a new philosophy in maintenance and diagnostic programs will be offered. The PDP-9 Maintenance Package is designed to allow the customer to pin-point possible failures to the individual card — and in some cases to the function of a card — in a matter of minutes and without using an oscilloscope. Starting with several easily-tested assumptions about the Control Memory, the PDP-9 Maintenance programs check each computer function in order and in a pattern designed to yield a maximum amount of information as to the source of possible trouble.


PDP-9

BIG POWER FOR RESEARCH AND ENGINEERING

The PDP-9 gives the research scientist big computer power under his direct control and the systems designer a truly powerful control facility.

Physical Sciences

The PDP-9 has a special capability in the physical sciences. In physics, for example, special PDP-9 Multi-analyzer configurations are available. PDP-9 programs are available to input pulse height analyzer data. The PDP-9 can directly control the cathode ray tube display formats including single parameter with markers, integration under peaks, curve calibration in mev., dual parameter isometric, contour, and lined display. Data may be punched on paper tape or written on DECtape or IBM compatible magnetic tape.

In chemistry, the PDP-9 can be interfaced to gas chromatographs, mass spectrometers, NMR spectrometers, or x-ray diffractometers to speed up the collection of data and enhance its interpretation.

Life Sciences

DEC has pioneered the application of computers in life science laboratories for on-line experimental research: These computers are not only used to reduce data, but also to control experiments, to selectively acquire data, and to display data in time for the researcher to creatively vary experiment sequences and parameters based on emerging results. The PDP-9 is designed to fit in the laboratory environment. It is fast enough to accept the experimental data as responses are generated by living organisms, large enough and powerful enough to do large scale calculations in the laboratory, yet compact enough to exist side by side with the experiment.

Earth and Space Sciences

The PDP-9 also gives the earth and space scientists a new, powerful tool for data acquisition and analysis. Like its PDP brothers already at work in these fields, it can be used to collect and analyze seismic signals, track signals in space, or plumb the ocean depths for oceanographers.

Other applications for which the PDP-9 is particularly suited include:

- Systems and process control.
- Computer aided design and other computer controlled cathode ray tube display programs.
- Hybrid computation, including simulation.
- High speed data collection.
- Data communications and message switching.
- Development of software and instruction in the computer sciences.
- Testing.

The PDP-9 may be connected to large time-sharing systems as a powerful computer based remote terminal or perform as a free standing general purpose data processor and problem solver.


PDP-9
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ND
NUCLEAR DATA
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